THE UNIVERSITY OF ALBERTA

DIGITAL TO ANALOG CONVERTER

by

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled Digital to Analog Converter submitted by Kenneth T. Thorsen in partial fulfilment of the requirements for the degree of Master of Science.

ABSTRACT

This thesis deals with the design of a decoder for conversion of digital information to its equivalent analog representation.

A conventional flip-flop register provides reference voltages for a ten bit binary weighted network and also acts as a hold circuit for conversion rates up to one hundred thousand words per second. Input gates to each flip-flop sets the state of the flip-flop to correspond to the input code information and prevent the flip-flop from changing state unless the code input is different than the preceeding bit.

The unipolar weighting network voltage is passed through a gated differential amplifier to give positive or negative output voltages in response to information carried by a sign bit.

The constructed decoder is to be used in conjunction with an encoder and memory to provide a pure time delay which is necessary in many analog computer problems.

ACKNOWLEDGEMENTS

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INTRODUCTION

One of the problems encountered in analog simulations is that of providing a time delay. The pure time delay, or transport delay, occurs in many problems of physical significance. A signal subject to a pure time delay is reproduced exactly in shape but is delayed in time. In the frequency domain the pure time delay has the following property; all sinusoidal components of the input signal are reproduced exactly in amplitude but have a phase shift proportional to frequency.

A few examples where a delay may be required are:

(1) Process control.

(2) Problems containing the dynamics of a human operator.

(3) The simulation of the behavior of economic systems.

For iterative problems the storage of information for use at a subsequent time can also be provided by a time delay.

Some of the methods(1) of obtaining a time delay are listed along with a brief discussion of them.

(1) Delay Lines

Delay lines generally prove to be practical for delays in the order of micro-seconds or milliseconds but flexibility is somewhat limited.

(2) Magnetic Recorders

Magnetic recorders are capable of handling a much wider range of time delays. Amplitude modulation, which is normally

used at lower frequencies, is subject to the disadvantage of sensitivity from section to section of the tape. This appears as modulation of the carrier and, hence, introduces error. Frequency modulation removes this objection but any variation in tape speed appears as frequency modulation which also causes errors. For the case of variable delays, special modulation techniques must be applied to prevent amplitude distortion.

(3) Electromechanical

The basic elements for electromechanical delays are switches and storage capacitors. The accuracy depends on the quality of the storage capacitors and the current available to charge these capacitors to the input signal value in required minimum time. The relay type delay essentially consists of an operational amplifier sample-hold circuit. Its main disadvantage is the large number of operational amplifiers required.

The capacitor disc delay is a rotating wheel upon which holding capacitors and charging contacts are mounted near the circumference. As the disc rotates an input contact charges successive capacitors to the input signal value. A second contact reads out these values after a finite delay, the length of the delay depending on the physical distance between input-output contacts and the speed of rotation of the disc.

For uniform delays the speed of rotation of the disc must be well regulated.

(4) Simulation with analog computer components

The fourth method makes use of conventional analog-

computer components to synthesize an approximate time delay circuit. Three such approaches are:

(a) Padé expansion.

(b) Bode expansion.

(c) Experimentally synthesized circuits designed at Westinghouse.

These involve the mathematical expansion of e^{-st} and simulation on the computer. All three methods may be extended from the case of a constant delay to that of a variable delay.

In the Padé case it is relatively simple to derive the partial fraction approximation but the subsequent factoring to permit easy simulation is difficult to carry out. Thomson suggests a method which avoids factorization and simplifies the procedure somewhat.

In the Bode case the factorial form is used directly, but the optimum values of the parameters are determined by derivatives of the phase function, followed by the solution of a set of simultaneous nonlinear algebraic equations. This can become quite tedious.

Stubbs and Single of Westinghouse Electric Corporation have carried out extensive investigations of variable and fixed time delays. In contrast to the previous methods, the number of amplifiers required is reduced at the expense of flexibility, by employing passive elements.

Low-pass networks which are easy to synthesize can be used to approximate the pure time delay but their frequency and phase characteristics are poor compared with the above

networks.

The track and hold delay could include such methods as the relay type. Electronic switching can replace the relays, enhancing upper frequency limits of input signal, but a large number of amplifiers are required.

(6) Digital Techniques

Digital techniques provide another method of generating a time delay. The analog voltage is sampled at a higher frequency than its highest frequency component, changed to a coded value which can be stored for the required delay in a memory, then extracted and converted back to the original form. Accuracy of reproduction of the analog signal depend on the encoding and decoding process, assuming no information is lost in transfering from encoder to memory and memory to decoder. Errors result from quantizing the original signal, but the magnitude of these errors can be kept small if the quantized steps differ by only a small fraction of the overall voltage level to be encoded. The larger the ratio of sampling frequency to the highest sinusoidal component in the input signal, the better the reproduction. This same conversion unit could be used as a link between the analog and digital computer and vica-versa. The design of a portion of a digital time delay is to be the basis of this thesis. The time delay unit can be conveniently represented by the following block diagram.

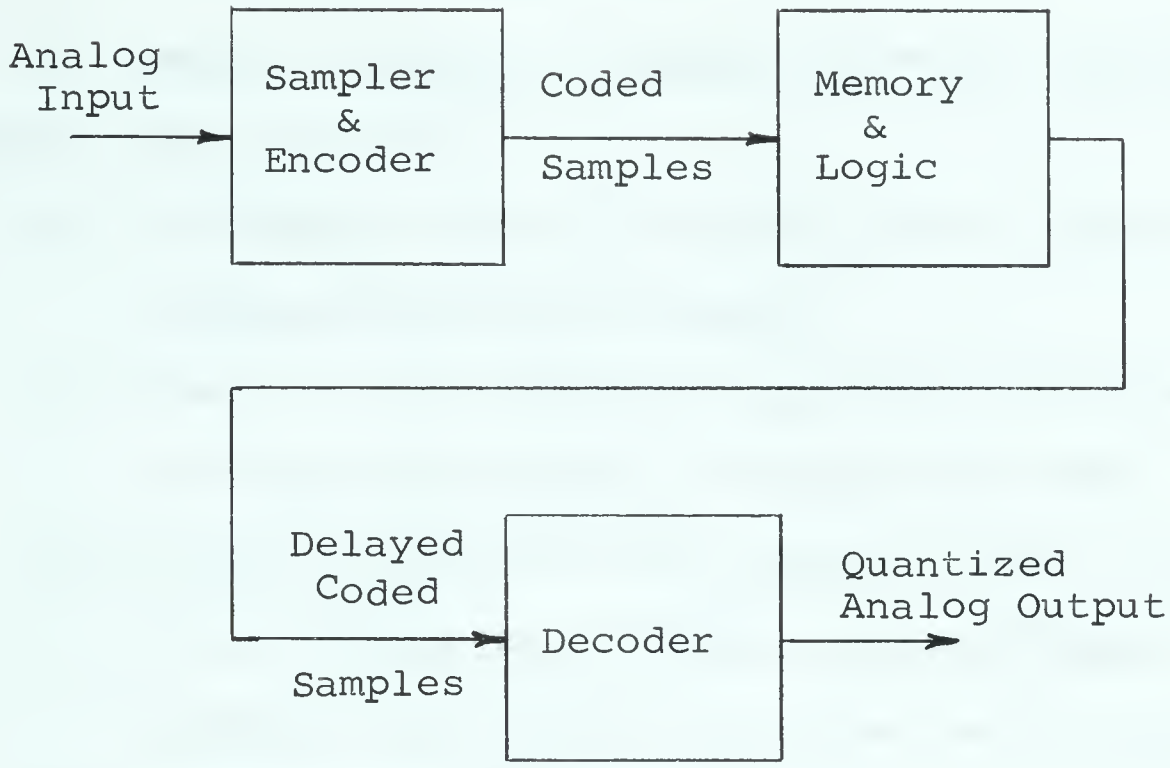


FIG. 1 DIGITAL TIME DELAY

The three sections shown, encoder, memory and logic, and decoder are to be designed and constructed as three separate projects. This thesis deals with the decoder (conversion from digital to analog).

STATEMENT OF PROBLEM

To design a digital to analog converter with the following specifications.

(1) Conversion rate to be from zero to one hundred thousand words per second.

(2) Zero to one thousand steps binary plus one bit for sign thus making an eleven bit word.

(3) Plus or minus 10 volts maximum output so that it is compatible with Pace Analog-Computer (using a gain of ten amplifier on the Pace).

(4) Input logic to decoder

Logic 0 —— 0 volts

1 —— -5 volts

Sign Bit 0 —— positive output voltage

1 —— negative output voltage

(5) All circuits to be solid state.

(6) Clock pulses if required are available.

(7) Power supply voltages to be chosen in conjunction with requirements for encoder and memory.

(8) Type of code to be acceptable to encoding process.

(9) Code available in parallel form and bit pulse width approximately two microseconds.

DIGITAL TO ANALOG CONVERTERS

For digital to analog conversion the same technique is generally applicable for all digital-to-voltage or digital-to-current converters, although some variations exist. Fig. 2 shows a typical decoder in block diagram form.

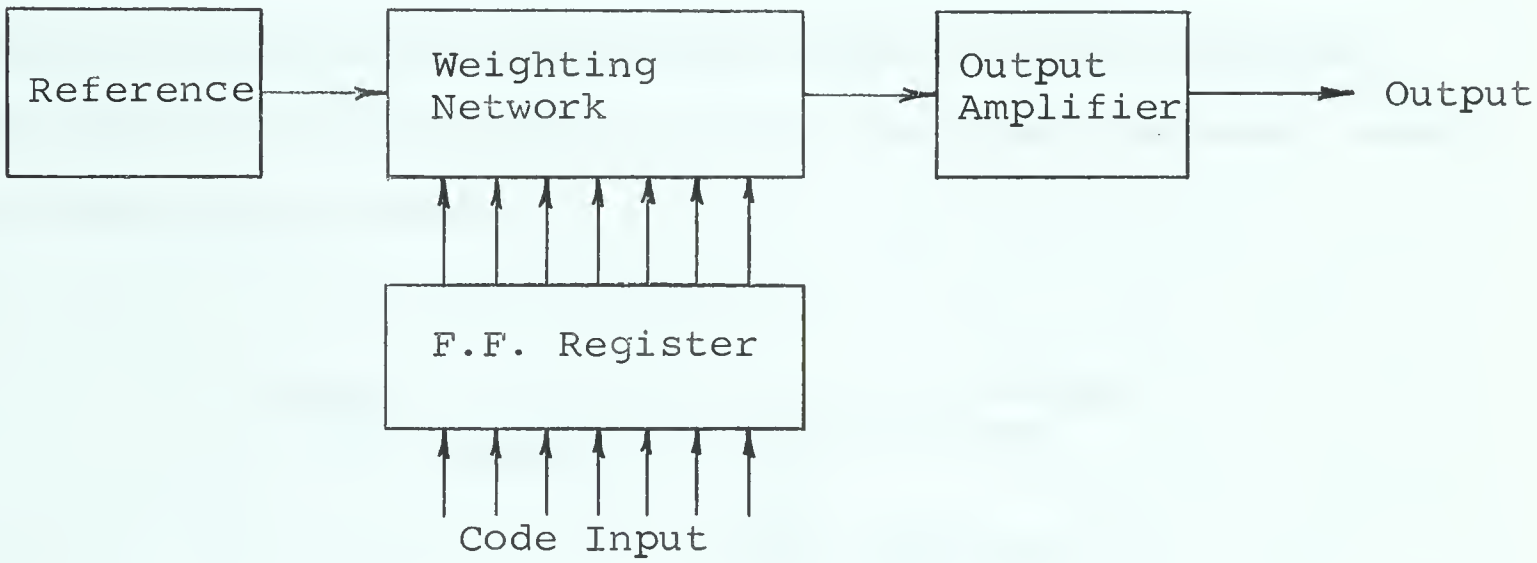


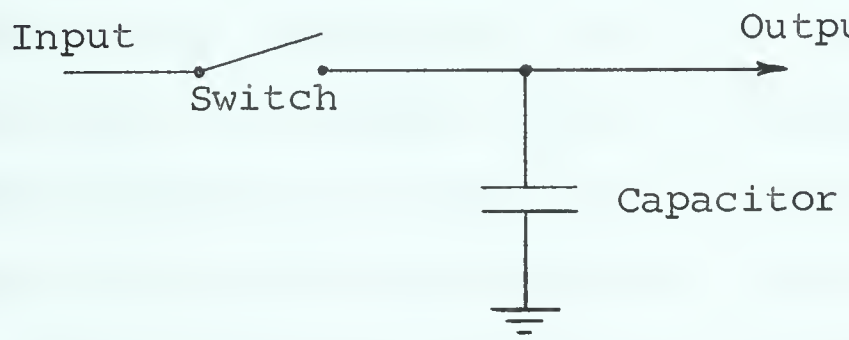
FIG. 2 TYPICAL DECODER

The flip-flop register holds the digital number. The output from the flip-flops control two well defined voltage levels which are obtained from the reference. Either one or the other of the reference voltages is applied to the divider network depending on the code input bit being a zero or one. The divider network is weighted so that each bit of the register will contribute to the output in proportion to its value. Since the divider network is simply a passive network, the digital input signal determines the analog output voltage. The output amplifier provides a buffer between

weighting network and load.

Although the decoder in Fig. 2 contains the essential components for a converter, some of the following points should be considered.

Since code information is received intermittently some type of hold device is required to insure that the decoded quantity remains at the output of the decoder until a new value is read in if a quantized output is to be obtained. The preferred hold circuit acts as the ideal component shown in the circuit below.



IDEAL HOLD CIRCUIT

When the switch is closed the capacitor charges instantaneously to the input signal value and then follows the input. When the switch is opened the capacitor holds the voltage value it had at the instant of opening.

The hold circuit in a decoder is not necessary in all types of devices. The output can be a pulse amplitude modulated signal which is passed through a low pass filter to obtain an analog output voltage. This type of digital to

analog converter is more applicable to a fixed conversion rate because the output from the filter would depend on the pulse repetition rate and its duty cycle. A technique(2) using pulse width modulation can also be employed but again its usefulness as a variable rate decoder is limited. The code is required in serial form for the above converter and since this project gives specifications for parallel code no further discussion will be presented on serial type decoders.

To obtain both positive and negative voltage outputs, a voltage can be added to the analog input to the encoder so that voltages of one polarity are encoded. This voltage may be subtracted from the decoder output to produce the original signal. This eliminates the plus-minus sign bit. If the analog signal is rectified and encoded, a circuit must be included which will produce a positive or negative analog output voltage in response to the information carried by the plus-minus sign bit. Although this circuit is not shown in Fig. 2 it could be a part of the output amplifier or be included along with required logic to provide a positive or negative reference voltage for the weighting network.

Design Considerations

The following system parameters must be considered in converter designs.

(a) sampling rates

(b) quantization levels

(c) choice of code

(d) conversion time

(e) holding requirements

(f) complexity of equipment

(g) reliability

The Sampling Theorem may be stated as follows(2): "It is necessary to take more than two points per cycle of the highest frequency component in a signal in order to recover that signal". An n-bit binary decoder has 2^n discrete output states evenly distributed between two reference potentails. The analog voltage may therefore contain an error equal to one quantization level, with the magnitude of the error decreasing as the number of bits is increased. The number of quantization levels and the sampling rate therefore dictate the maximum possible accuracy of reproduction of the original analog signal. For this particular decoder these two parameters were given as project specifications.

The type of code used must be acceptable to the encoding process. Binary code seemed most practical thus the type of code is also considered as a given parameter for the digital to analog converter.

The maximum conversion rate is theoretically limited only by the minimum time between read-ins to the converter flip-flops and can easily be in the megacycle range, however, the desired ratio of settling time to non-settling time usually determines the maximum usable conversion rate. The

settling time of a converter is measured from the time the digital read-in is performed to the time when the analog output has settled to within specified limits of accuracy.

The conversion time must be no longer than the maximum sampling rate will allow and the ratio of conversion time to time between read-ins will have a profound influence on the type of holding requirements. The holding requirements will also depend on the quantization levels and the sampling rates since this determines the maximum allowable tilt and maximum hold time. If the tilt due to holding approaches the value of a quantized step, the advantage of having a large number of steps no longer exists.

In Fig. 2 the flip-flop register can be used as the holding device if the read-in of a new word does not produce undesirable effects in the output during the transition to the new analog value.

High frequency switching transients will occur at the output of the weighting network but these may be of no significance if the output amplifier does not respond to them. If these switching transients are passed by the output amplifier, holding may be required during the read-in of a new word. If this is necessary a capacitive or other type hold can be used so that the new analog quantity can not appear at the converter output until switching transients have subsided.

In practice, capacitor holds have a finite charge

time and leakage causes the voltage to decrease during the holding period. Therefore, at low switch repetition rates voltage tilt is minimized by using large value capacitors. At high repetition rates, the current required to charge the capacitor to the input signal level in allotted time could become excessive, therefore, a compromise between capacitor size and allowable tilt must be made. If switching transients can be ignored, using the flip-flop as a hold device is superior as it does not exhibit the tilt associated with capacitor holds.

The settling time is basically a function of the magnitude and duration of the switching spikes at the output of the weighting network and the output amplifier response. If holding is used during the read-in of a new word or if the output amplifier filters the switching transients occuring at the weighting network output, then settling time will essentially be that of the amplifier.

The previously mentioned switching transients are caused by variations in transition times of the register flip-flops. Also, flip-flops normally have a slower fall than rise time. Transient current drawn from the reference supply may cause momentary changes in the reference voltage thereby adding to switching disturbances. For weighting networks of the ladder type, signals must propagate through the ladder, therefore, giving additional variations in bit information arrival times at the output. This is not the case with binary weighted networks. For minimum spiking

care must be taken in selecting the proper input stages to the weighting network.

Items (a) through (e) determine in part the complexity of equipment as does reliability. The simplest system with maximum reliability is usually the designers goal and this will be considered during decoder design.

Considering the preceding discussion, design objectives, and the many possible variations in units that might adequately comprise the building blocks for a decoder, the circuit given in Fig. 3 was thought practical.

Details of actual components used will be included in the design section. Only a description of the operation of the decoder and requirements of individual building blocks will be given here, along with the reasons for the type of building block chosen.

With a conversion rate of zero to one hundred thousand samples per second, flip-flop holding seems mandatory. If switching transients can be minimized and are of a much higher frequency than the maximum sampling rate, they can be assumed negligible. This places fairly stringent requirements on the flip-flops. If turn on delay and turn off delay can be made equal as well as having extremely fast rise and fall times the spikes at the weighting network output should be fairly high frequency and easily filtered. To insure uniform triggering points, all changes in the state of a flip-flop will be initiated by a clock pulse. This is desirable since the clock signal can be obtained from a single amplifier.

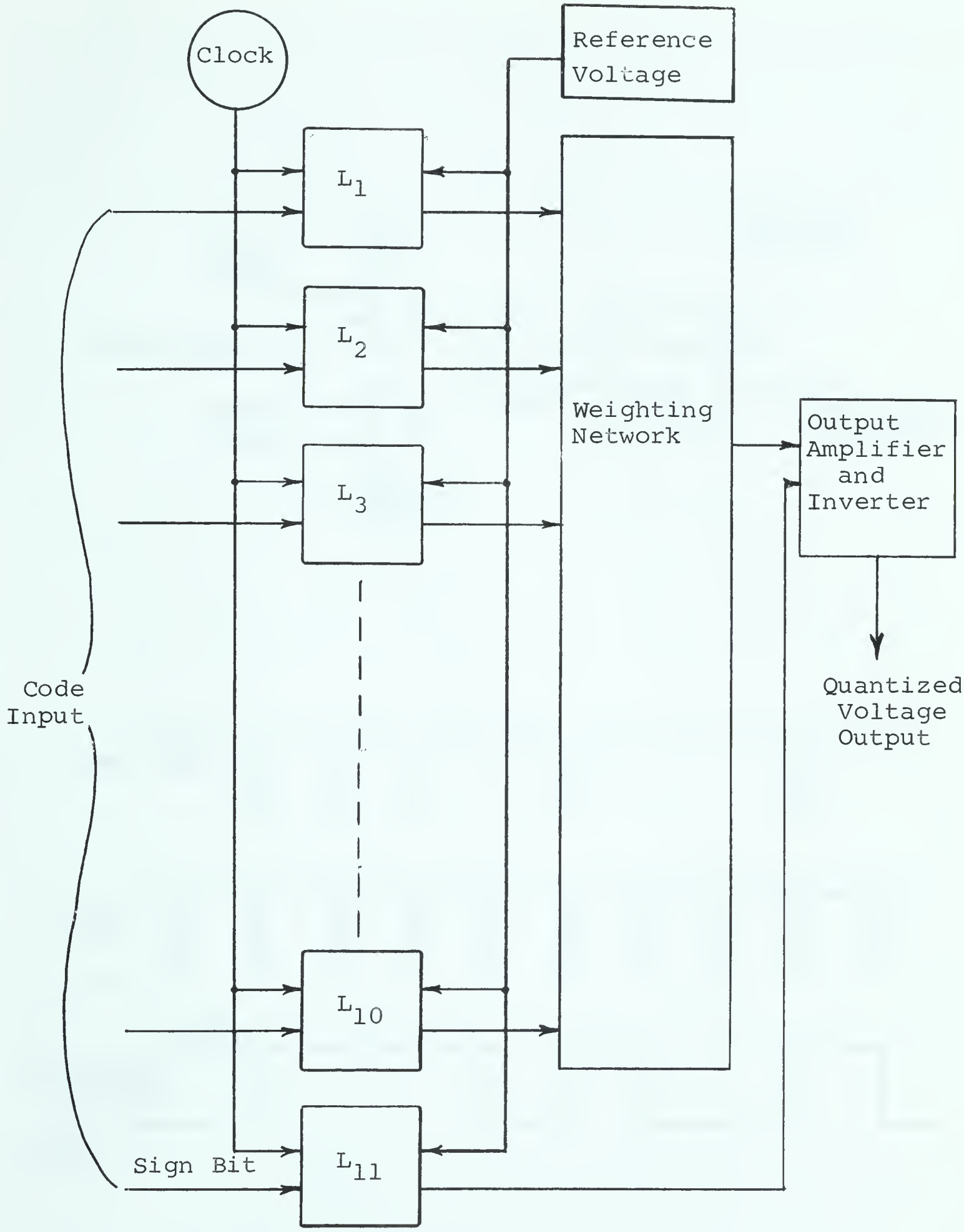
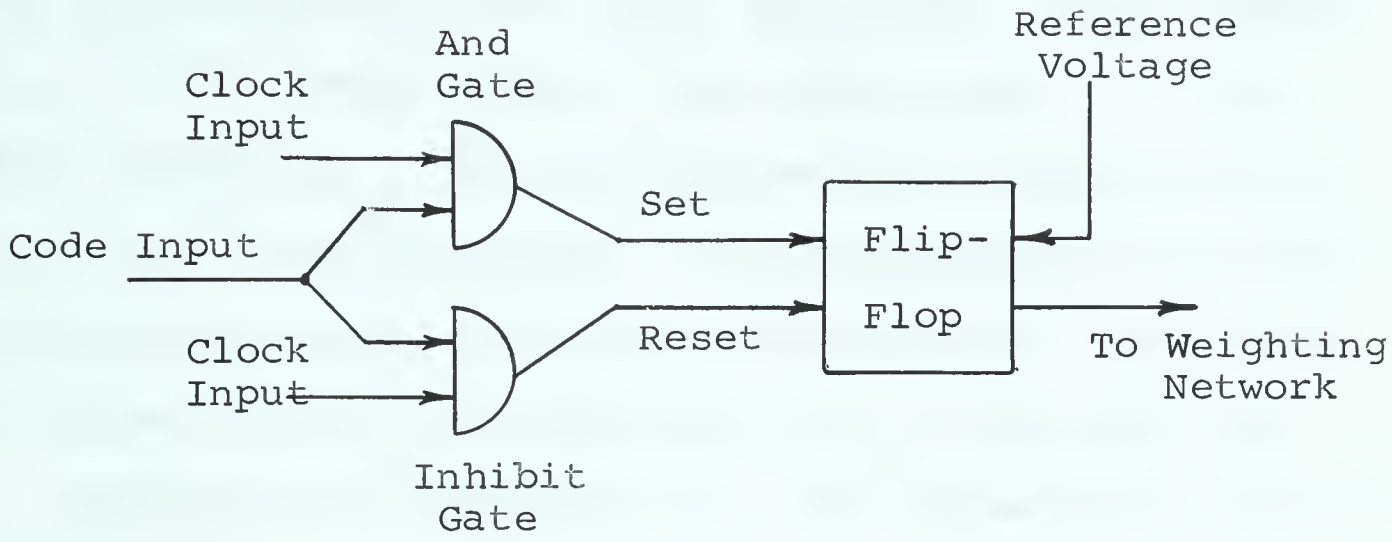


FIG. 3 DIGITAL TO ANALOG CONVERTER



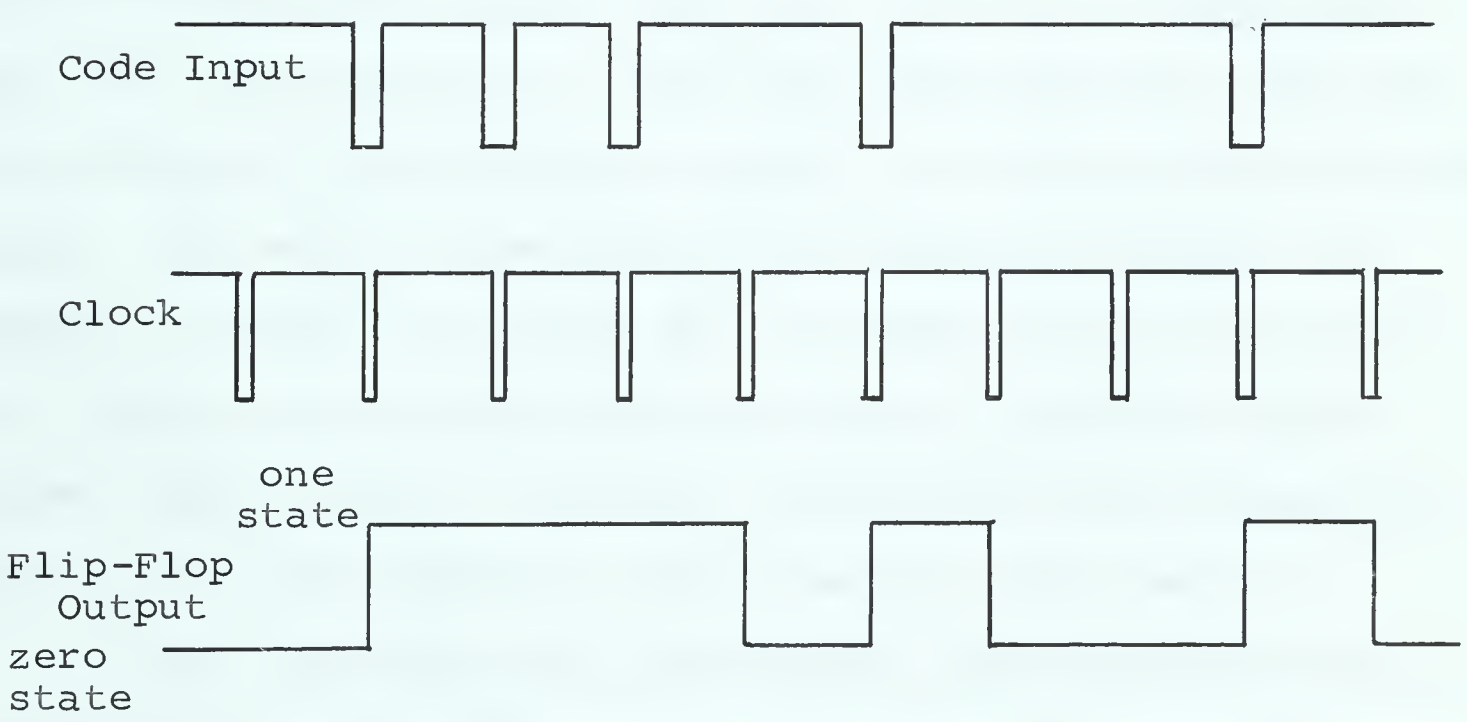


FIG. 4 LOGIC BLOCKS L_1 TO L_{11}

The code input pulse cannot, therefore, introduce a possible source of delay in switching of some flip-flops. Fig. 4 shows the flip-flop and associated input gates for setting and resetting the flip-flop to the "one" and "zero" states respectively. If the leading edge of the clock pulse is to be used for triggering it must be delayed with respect to the leading edge of the code pulse. The coincidence of a clock and code pulse at the "and" gate will allow the clock pulse to be transmitted to the flip-flop to set it in the "one" state. Meanwhile the presence of a code pulse at the inhibit gate will prevent the clock signal from resetting the flip-flop to the zero state. In the absence of a code pulse the "and" gate is inoperative, but now the clock pulse is transmitted through the inhibit gate for resetting. Therefore, only the coincidence of a clock and code pulse will set the flip-flop and the absence of a code pulse will allow it to be reset. The mode of operation of the gates minimizes the number of times a flip-flop has to change state since they will remain in a single state as long as successive code pulses are the same, therefore, eliminating the process of setting all flip-flops to "zero" before a new read-in.

The flip-flops will also supply the two reference voltages for the weighting network inputs. The upper level or "one" state will be obtained by clamping the flip-flop output through a diode to a well regulated reference supply. The collector-emitter saturation voltage will set the lower level or "zero" state. The accuracy of the upper level out-

put must be considered on the basis of how well the diodes can handle variations in clamp current, changes in voltage due to temperature fluctuations and the degree of matching between diodes for each flip-flop. The lower level voltage may also change as it is a function of collector current and temperature. Matching of transistors is also necessary to maintain identical reference voltages as collector-emitter saturation voltage varies from unit to unit.

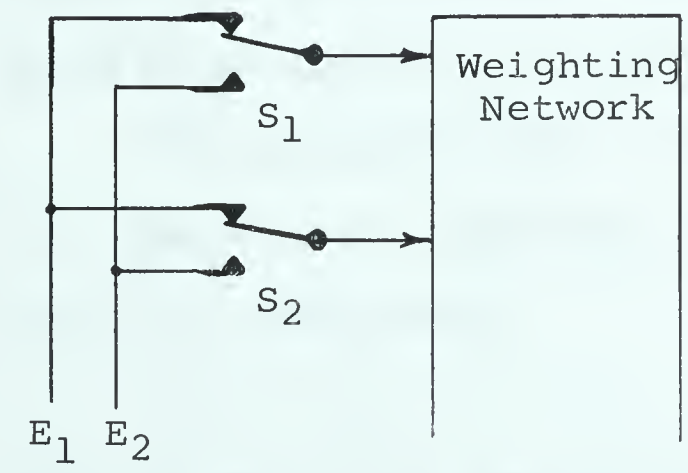
The choice of a weighting network is somewhat arbitrary as all types display desirable and undesirable qualities. The following discussion will give some of their characteristics, with additional information available in references(2).

Both speed and accuracy must be considered in determining the weighting network required for a specific application.

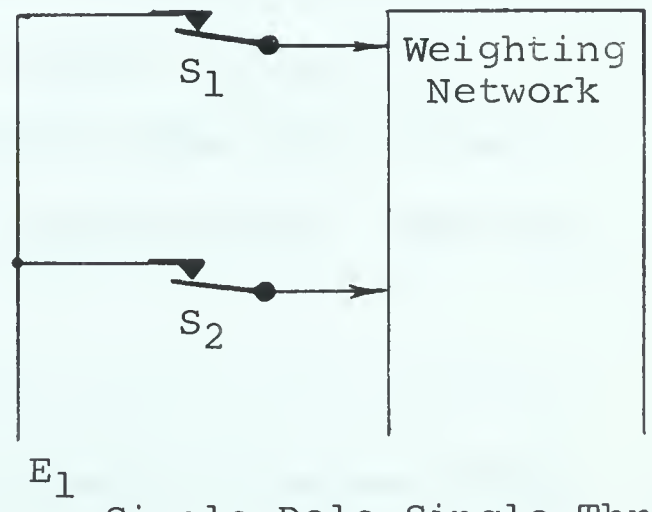
The binary weighted network with the equivalent of a single-pole double-throw switch is desirable because it presents a constant input impedance to the summing amplifier, therefore, making decoder accuracy independent of amplifier gain. The single-pole single-throw switch will only approach the same accuracy if the amplifier gain is infinite.

The ladder type network has the same inherent accuracy as the binary weighted decoder when considering the type of switch used as it only has a constant output impedance when used with the equivalent of a single-pole double-throw switch. The ladder network is superior so far as current

distribution is concerned, therefore, easing switch design. As an example, the ten bit binary weighted network current ratio of smallest to largest is 512:1 whereas the ladder current ratio is less than 14:1. The ladder network has a drawback due to unavoidable wiring capacitance between each resistor junction and ground. This causes a delay which increases from the most significant bit to the least significant bit. As a practical example, C.R. Pearman and A.E. Papodi(3) give a delay per bit of approximately fifteen nanoseconds for a five bit unit, on printed circuit board, with a characteristic impedance of ten thousand ohms. Perhaps at the maximum conversion rate required for this project the propagation time through the ladder would be of no consequence, but, to minimize any possible chance of enhancing switching spikes the binary weighted network was chosen. The large differences in bit currents, although not desirable, are not expected to present any problems.



Single-Pole Double-Throw Switches



Single-Pole Single-Throw Switches

The absolute accuracy of the weighting network depends on the absolute accuracy of the resistors; its binary accuracy on the resistors relative accuracy.

A digital converter reproduces exactly all the digital information which it accepts. Requiring monotonicity is one way to insure that all bits are meaningful. The converter is most likely to lose monotonicity when switching between values where all bits change state; for example, when changing from binary code 01111..... to 10000..... If the weighting of these bits is not quite correct the higher state might correspond to a lower voltage level.

The output amplifier provides isolation between the weighting network and load and provides a lower output impedance for driving these loads. Secondly in response to the plus-minus sign bit it must give a positive or negative output from a unipolar input. The amplifier must be D.C. and have a settling time less than one microsecond for step inputs to be able to satisfactorily handle signals at the highest conversion rate. Two of the possible configurations which might prove satisfactory are shown in Fig. 5.

The circuit shown in Fig. 5-(a) makes use of two D.C. operational amplifiers and a single switch. With the switch in position A;

$$E_o = -E_i$$

With the switch in position B the output is the sum of E_i plus $-2E_i$, therefore;

$$E_o = -(E_i - 2E_i) = +E_i$$

If the switch is controlled by the plus-minus sign bit the proper polarity voltage can be obtained.

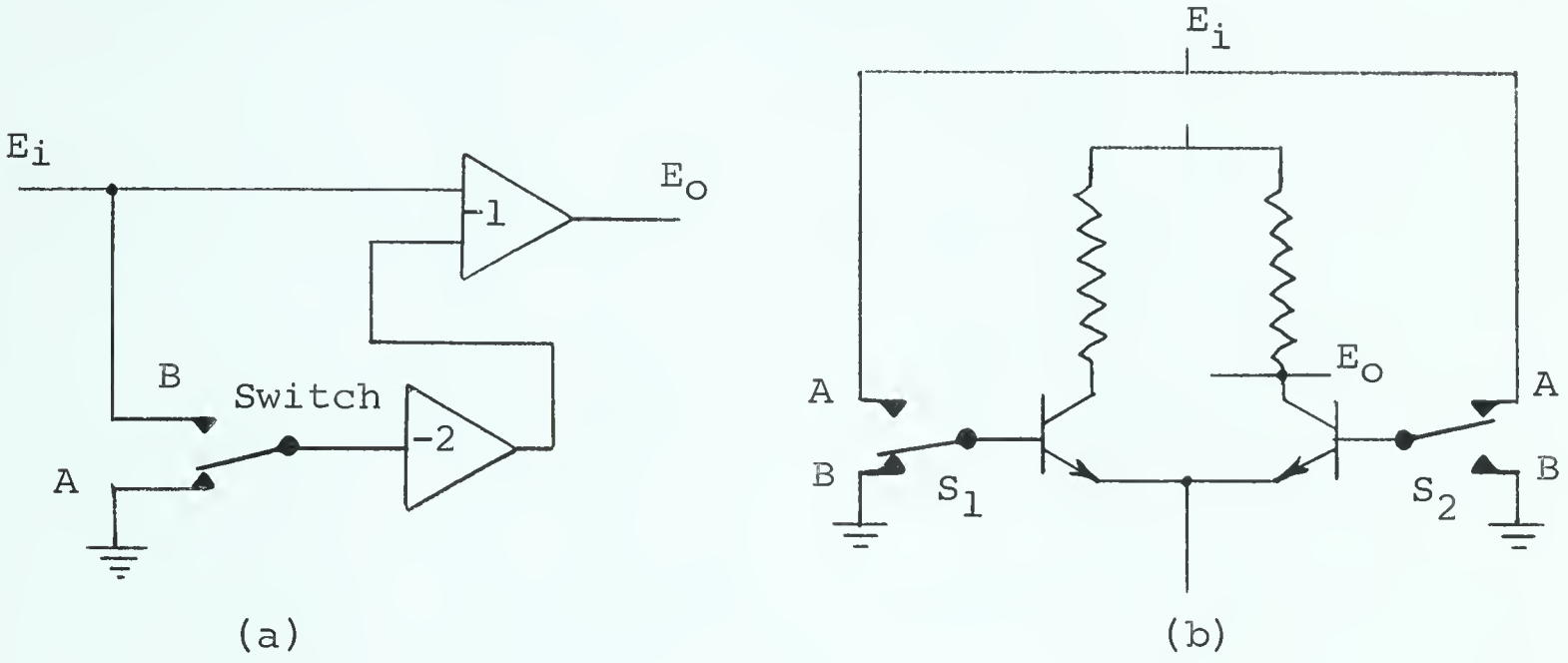


FIG. 5 INVERTING AMPLIFIERS

The circuit in Fig. 5-(b) make use of the characteristics of a differential amplifier. A differential amplifier gives as an output the difference between two input signals. With S_1 in position A and S_2 in position B;

$E_o = AE_i$ where A is the gain of the amplifier.

With both switches in the opposite position the output is:

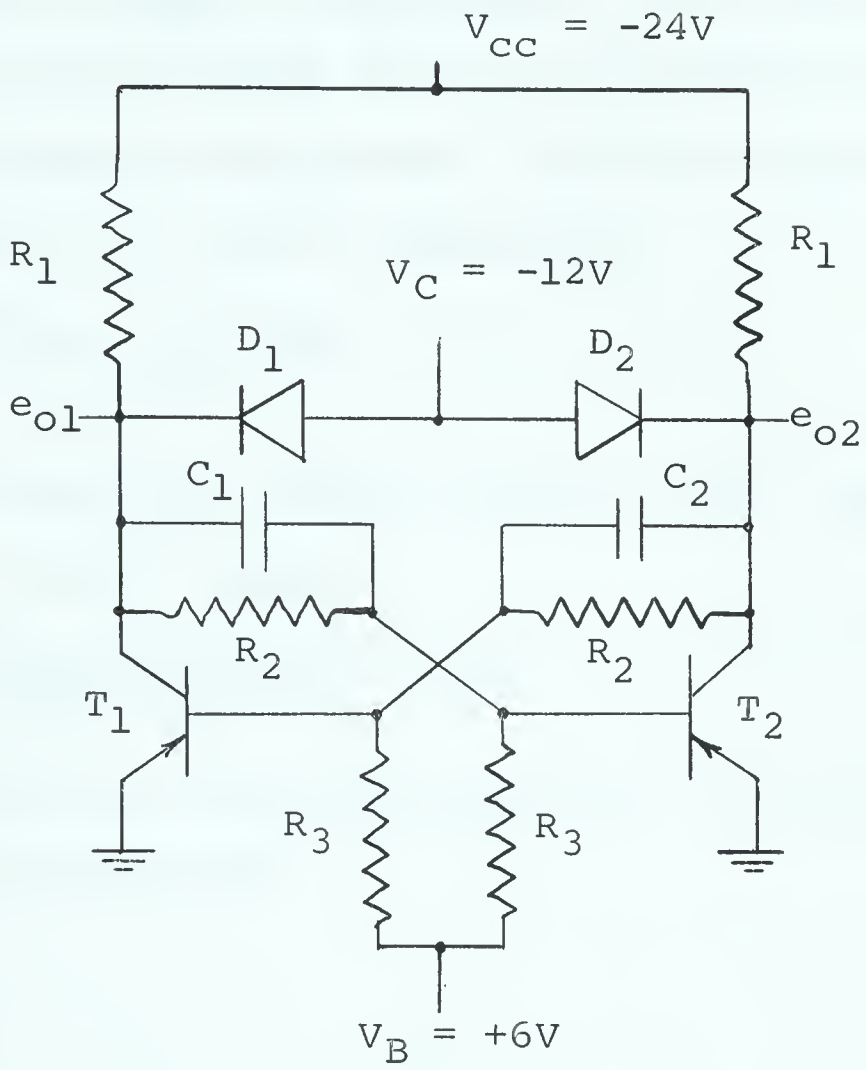
$$E_o = -AE_i$$

This amplifier can therefore be used to obtain an inverted or non inverted output depending on the position of S_1 and S_2. The difference amplifier may need additional output stages to give required output impedance.

The second method was chosen as it was thought to be simpler, cheaper and give equally good results.

DESIGN OF CIRCUITS

Saturated Flip-Flops with Clamped Outputs



$T_1 = T_2$ = 2N1309

D_1 = 0A10

D_2 = Any Germ. Diode (OA5)

FIG. 6 CLAMPED FLIP-FLOP

A well regulated minus twelve volt supply required in other parts of the time delay unit was chosen as the reference voltage. V_{CE} saturation provides the second reference level. The larger the value of V_{CC}, the more efficient the flip-flop since for large voltages the transistor collector saturation current will be approximately the same as the clamped current. Although a larger value might be more desirable, minus twenty-four volts was considered to be practical for the type of transistors chosen.

To maintain a relatively constant voltage drop across the clamp diodes for variable loads and small changes in V_{CC}, a large clamp current is desirable. For anticipated current changes through the clamp diode an acceptable minimum value of ten milliamperes was chosen. Ignoring current through R_2 - R_3, the value of R_1 can be calculated.

$$R_1 = \frac{V_{CC} - V_C + V_D}{I_C}$$

Where V_D is the diode forward voltage drop. Substituting for voltage and current values

$$R_1 = \frac{24 - 12 + 0.3}{10 \times 10 - 3} = 1.23K$$

To find the value of R_2 and R_3, the following equivalent circuits were used.

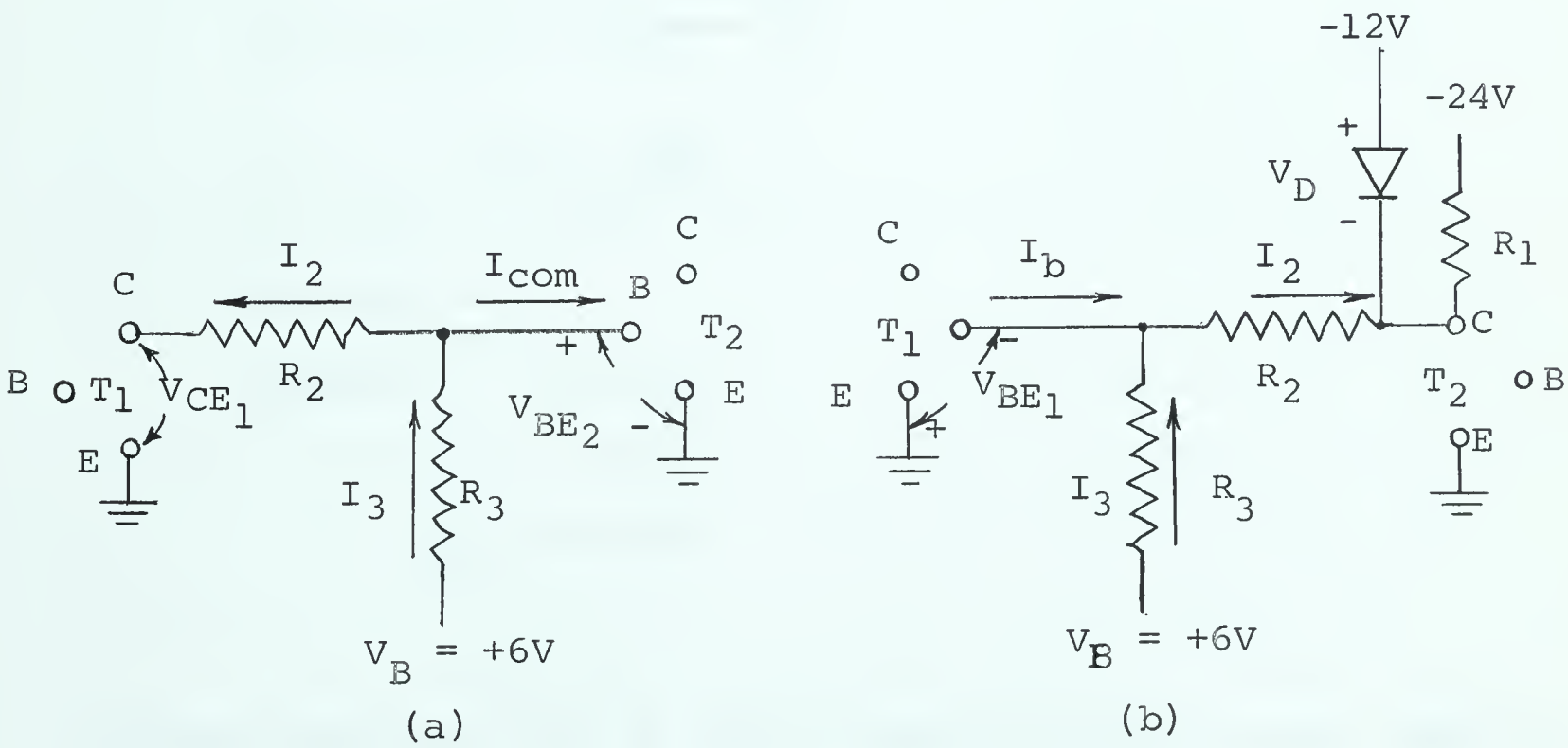


FIG. 7 FLIP-FLOP EQUIVALENT CIRCUITS

To insure that T_2 is cutoff (Fig. 7-(a))

(1) $I_2 = I_3 - I_{com}$

(2) $I_2 = \dfrac{V_{BE_2} - V_{CE_1}}{R_2}$

(3) $I_3 = \dfrac{V_B - V_{BE_2}}{R_3}$

where $I_{com} = .200$ ma

$V_{CE} = -0.3V$

$V_{BE_2} = 0.5V$

Eliminating I_2, I_3 and substituting for known values, equation (4) is obtained.

(4) $0.8R_3 + 0.2R_2R_3 - 5.5R_2 = 0$

To insure saturation (Fig. 7-(b))

(5) $I_2 = I_3 + I_b$

(6) $I_2 = \dfrac{V_C + V_D - V_{BE_1}}{R_2}$

(7) $I_3 = \dfrac{V_B - V_{BE_1}}{R_3}$

(8) $\beta I_b \approx I_c$

where $I_c = 20$ ma

$V_D = -0.3V$

$V_{BE_1} = -0.3V$

$\beta = 40$

Solving equations (5) to (8) in terms of known values equation (9) is obtained.

$$(9) \quad 12.0R_3 - 6.3R_2 - 0.5R_2R_3 = 0$$

Combining equations (4) and (9) the values of R_2 and R_3 are found to be 15.8K and 21.8K respectively. Closest available resistance values are:

$R_2 = 15K$

$R_3 = 22K$

To find the value of the cross coupling capacitors the mode of triggering must be considered as well as stray capacitance and desired switching times. Since turn-on and turn-off delay, and rise and fall times must be identical, if possible, the values of the cross coupling capacitors were found experimentally.

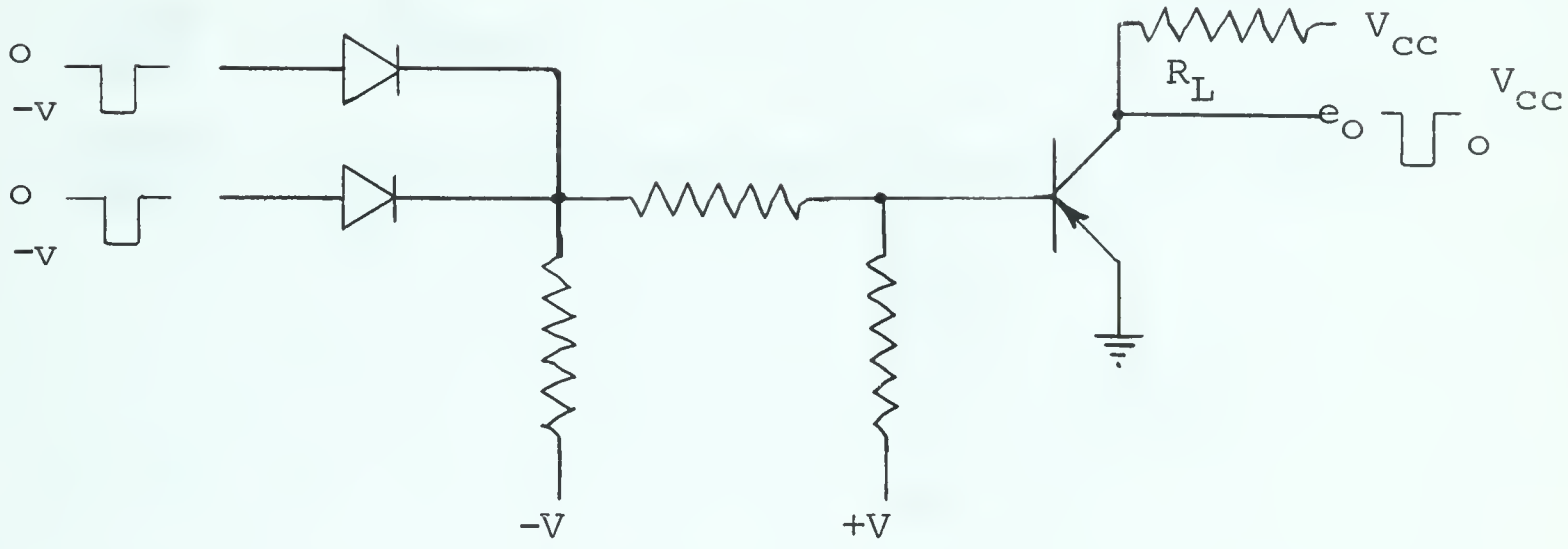
Gate Design

The presence of a code bit must set the output of the flip-flop to the "1" state and the absence of a bit must reset it to the "0" state. Also, only if the input bit is different than the preceeding one, should the flip-flop change state. This will give a minimum number of switching transients in the weighting network.

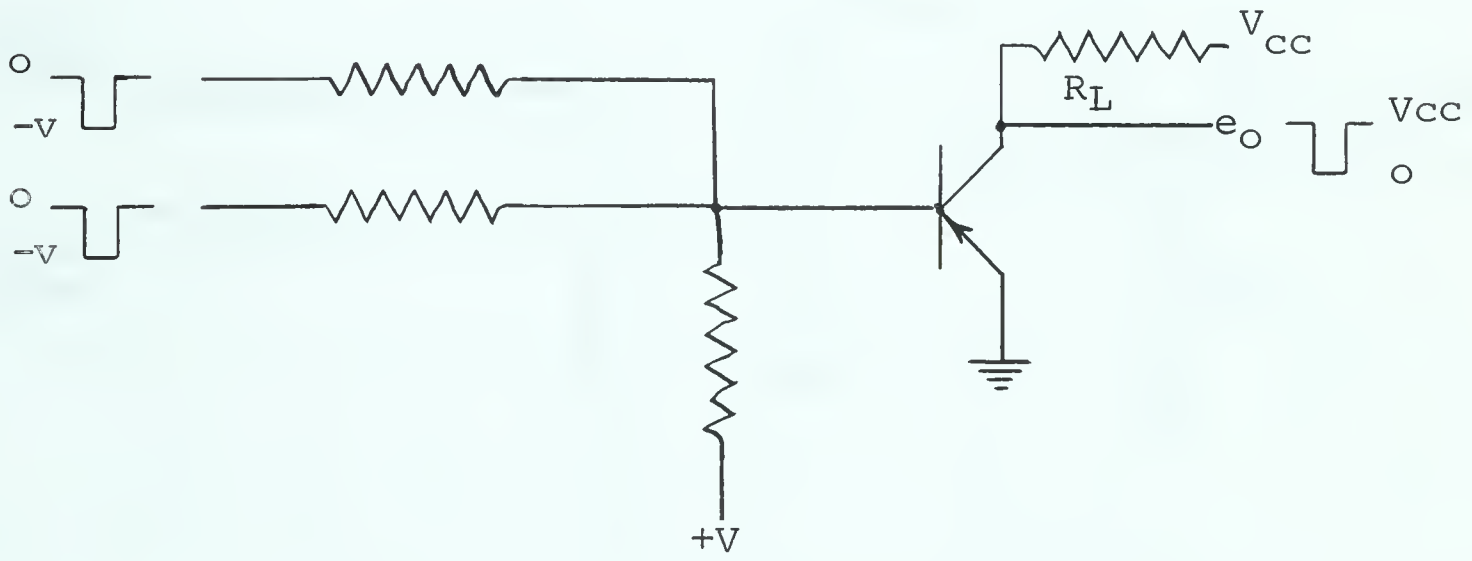
The use of transistors in the gate outputs would provide more power and insure more uniform flip-flop triggering points. The coincidence of a clock and code pulse sets the flip-flop to the "one" state therefore requiring an "and" gate. A choice exists between diode transistor logic, resistor logic or direct coupled transistor logic (Fig. 8). The circuit chosen for the "and" gate is shown in Fig. 9. Besides

the transistor, only three resistors and a single diode are required, compared to other gates shown. In Fig. 9, T_3 is normally off. A negative code pulse will appear at point A as a voltage equal to the forward diode drop if the clock input is zero. This will be transmitted to point B, but reduced in amplitude and not sufficient to turn on T_3. A negative clock pulse will reverse bias D_3 thus allowing the code input pulse to drive T_3 into saturation. If the collector of T_3 is tied to the collector of T_2 of the flip-flop, the gate is effectively coupled to the base of T_1 through the cross coupling capacitor. The value of C_2, therefore, determines the amount of energy available to switch T_1 and hence control its transition time from saturation to cutoff.

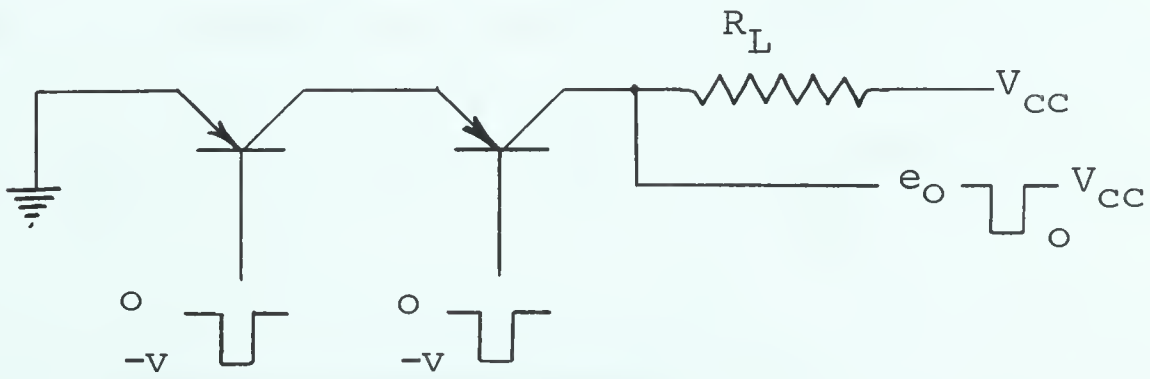
The reset gate must be able to trigger the flip-flop in the absence of a code pulse. The circuit shown in Fig. 10 meets this requirement. With both inputs at zero volts transistor T_4 is cutoff. A code pulse will make point D more negative therefore driving T_4 further into cutoff. The application of a clock and code pulse of equal amplitude will not change the potential of point D and the transistor still remains cutoff. If only a positive clock pulse is applied transistor T_4 will be driven into saturation. The resulting change in collector voltage is coupled through C_3 and D_4 to the base of flip-flop transistor T_1. The time required for T_1 to change from cutoff to saturation will depend in part on the energy available through C_3. If



(a) Diode And gate for negative inputs



(b) Resistor And gate for negative inputs



(c) Direct coupled And gate for negative inputs

FIG. 8 AND GATES

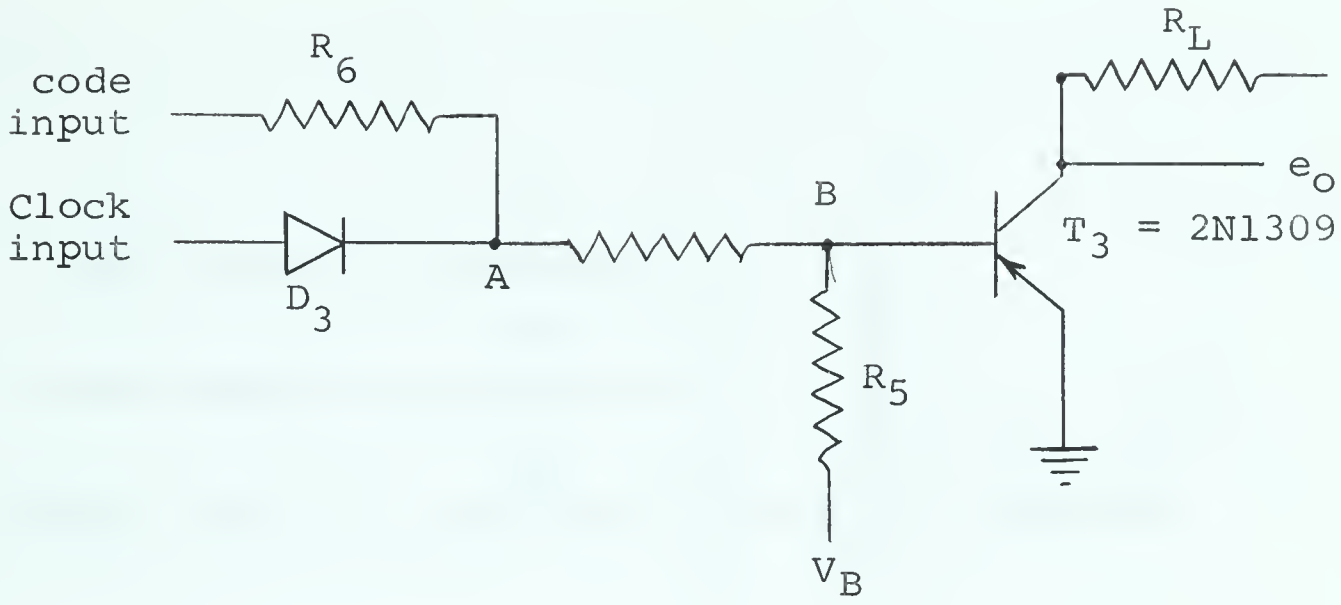


FIG. 9 AND GATE FOR NEGATIVE INPUTS

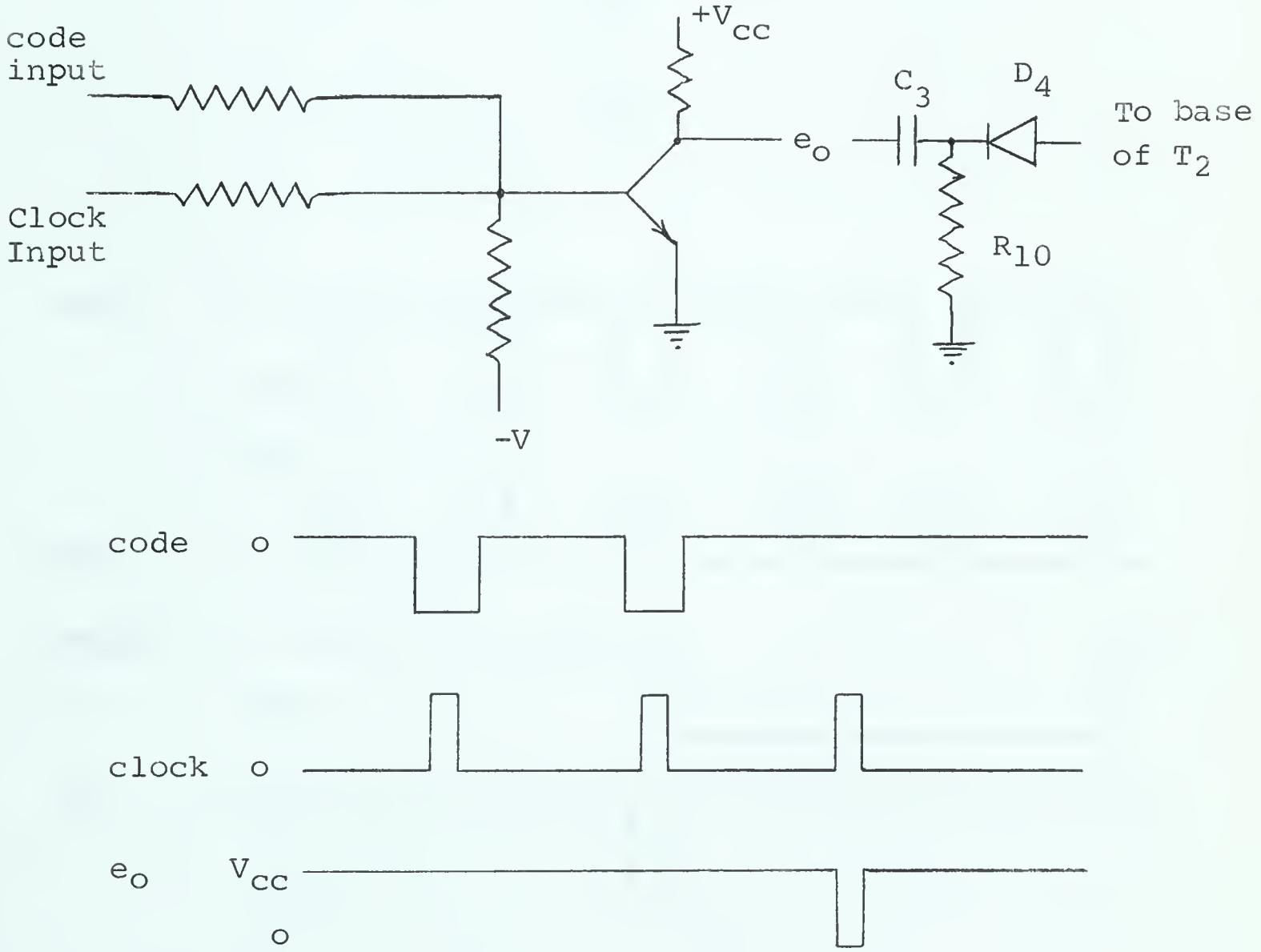
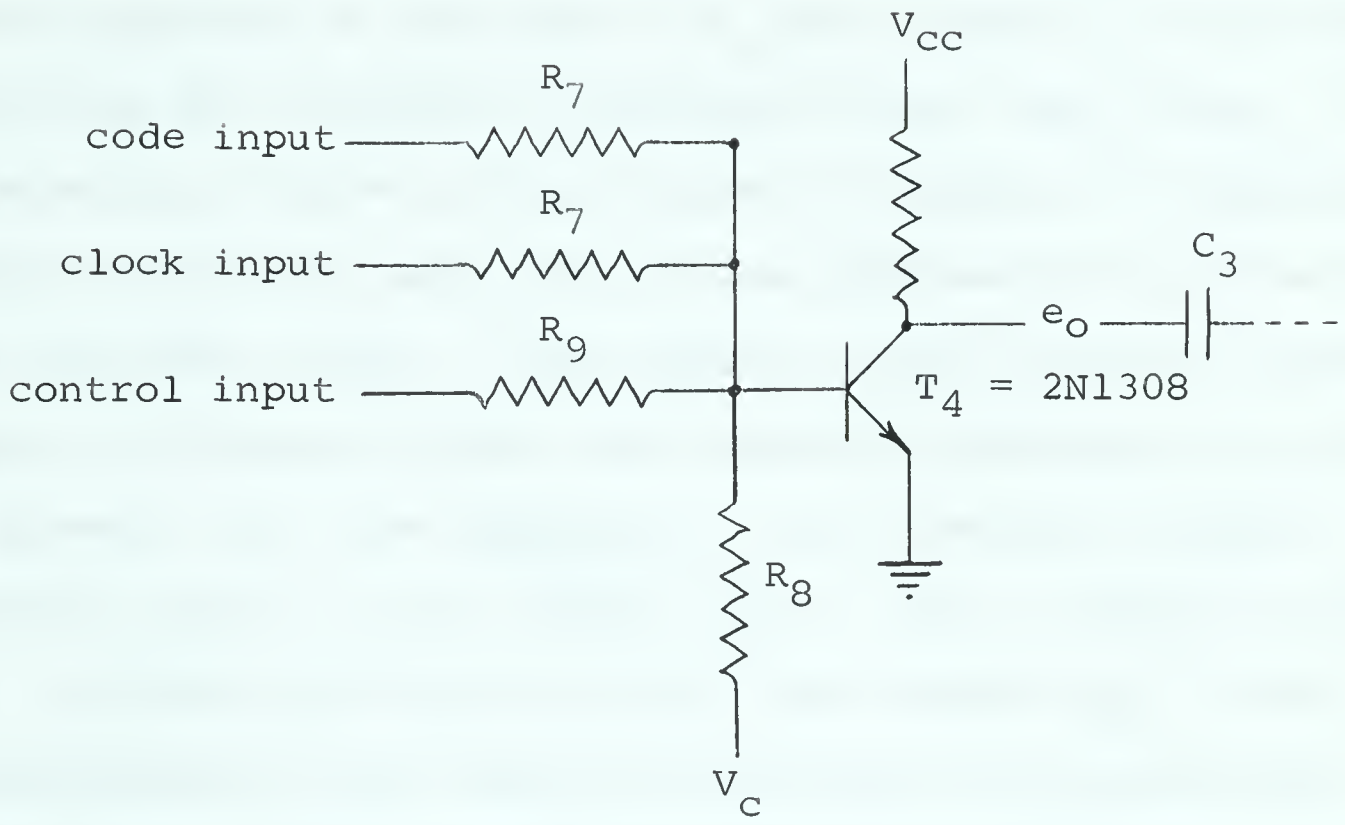


FIG. 10 INHIBIT GATE



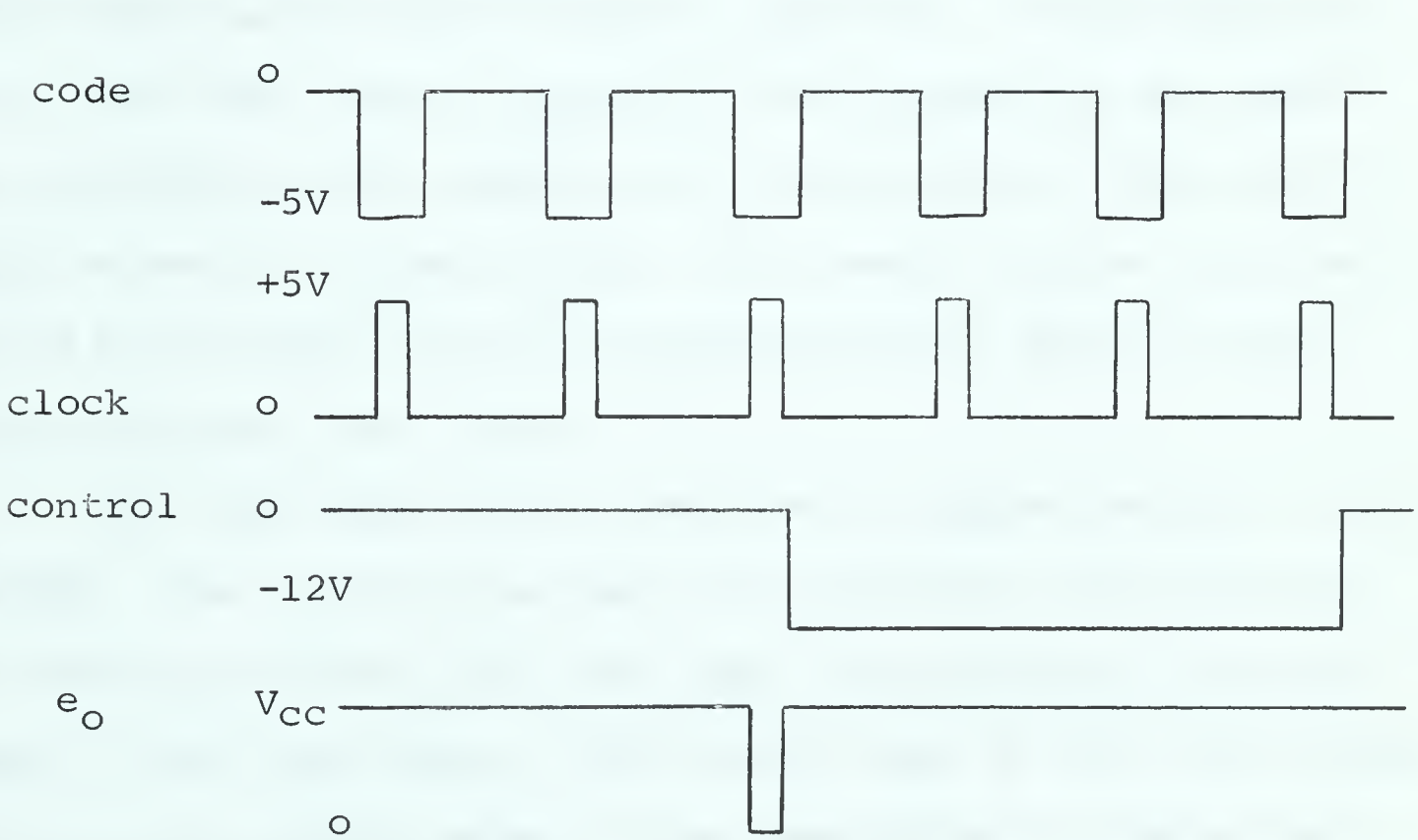


FIG. 11 CONTROLLED INHIBIT GATE

succeeding code pulses are absent the triggering pulse is still available at the base of T_1 even though it is not required as the flip-flop is already in the "zero" state. These unnecessary trigger pulses created a transient of approximately thirty millivolts amplitude and one microsecond duration at the flip-flop output. This appears at the weighting network output as unwanted signal and therefore introduces an error. To prevent this from happening it was necessary to add a "control input" to the inhibit gate. This is shown in Fig. 11. If the flip-flop is in the "zero" state (e_{o2} = -12V), a sufficiently large negative potential can be maintained at the base of T_4 to prevent it from saturating when a positive clock pulse and no code is applied. If the flip-flop is in the "one" state a positive clock pulse can now reset the flip-flop in the absence of a code pulse as the control input potential is zero volts. This means a pulse is transmitted to the base of T_2 for resetting only when the flip-flop is in the "one" state.

The code input pulse duration is approximately 2 microseconds. The clock pulse must be of shorter duration than the code pulse since the code input is inhibiting the clock input at the reset gate. The leading edge of the clock pulse must lag the leading edge of the code pulse to insure that switching is initiated only by the clock, therefore, the duration of the clock pulse was chosen as 0.6 microseconds.

Set Gate Design

State	Code	Clock	State of T_3
(1)	0	0	cutoff
(2)	0	1	cutoff
(3)	1	0	cutoff
(4)	1	1	saturated

TABLE 1

If the conditions stated in (3) and (4) of Table 1 are satisfied, (1) and (2) will necessarily be satisfied. For T_3 to be cutoff the circuit of Fig. 12 can be used. The equations for this circuit are:

(1) $I_5 = I_4 + I_{com}$

(2) $I_5 = V_B - V_{BE}$

(3) $I_4 = \frac{V_{BE} - V_D}{R_4}$

where $V_{BE} = 0.2V$

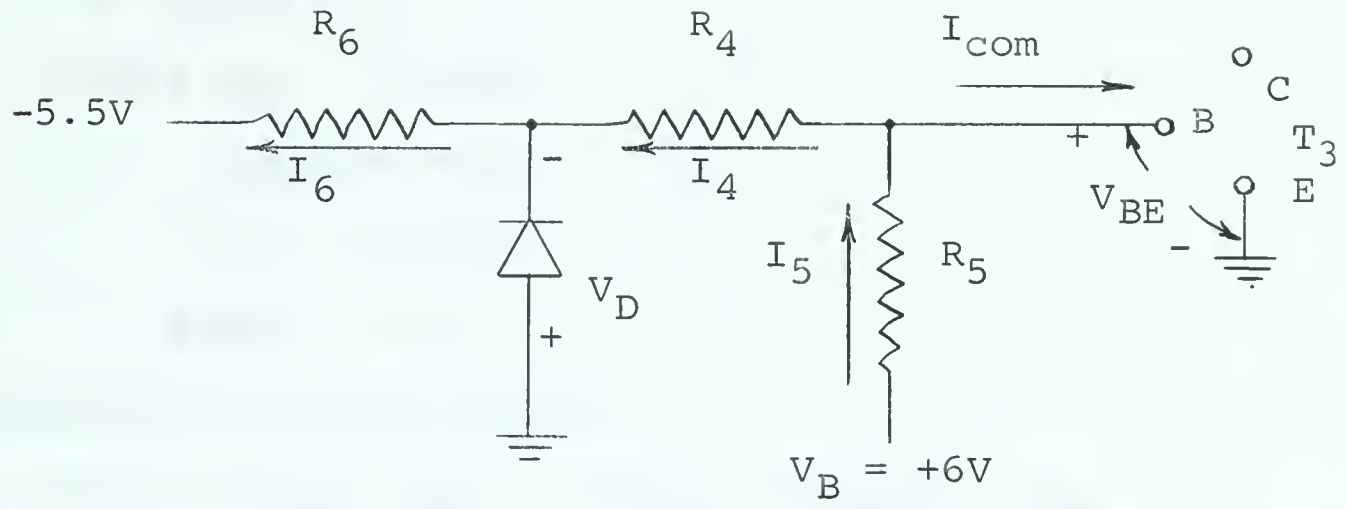
$V_D = 0.2V$

$I_{com} = 100 \mu a$

Solutions of the above equations and substitution of known values gives equation (4).

(4) $5.8R_4 - 0.1R_4R_5 - 0.4R_5 = 0$

Fig. 13 gives the equivalent circuit when T_3 is saturated. Assuming diode leakage current is negligible, equations (5) through (8) can be written.



Note: minimum code input = -4.5V

FIG. 12 EQUIVALENT CIRCUIT FOR "AND" GATE

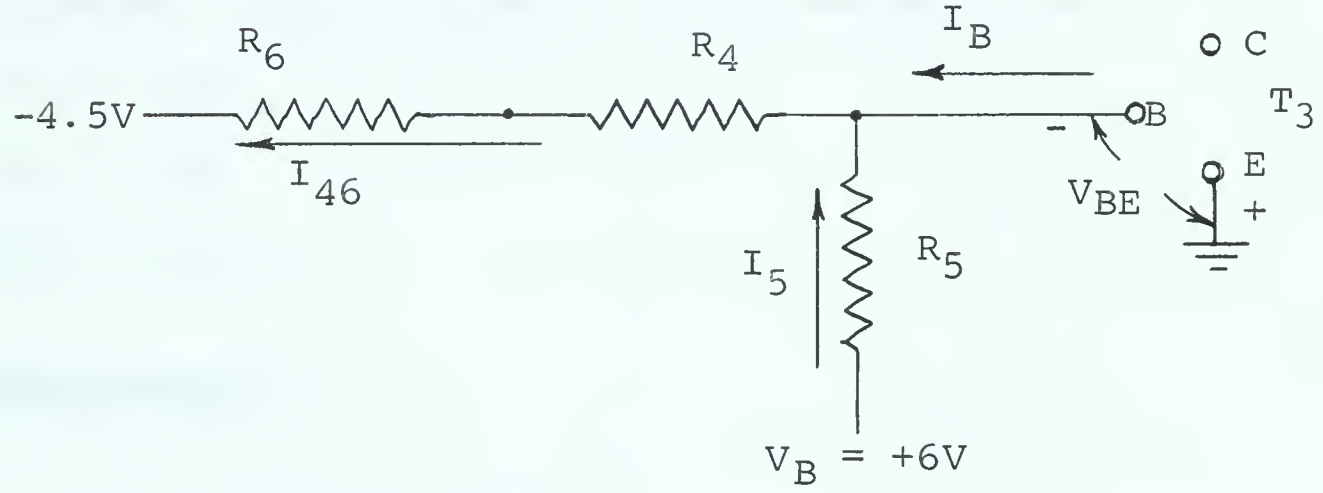


FIG. 13 EQUIVALENT CIRCUIT FOR "AND" GATE

$$(5) \quad I_B + I_5 = I_{46}$$

$$(6) \quad I_5 = \frac{V_B - V_{BE}}{R_5}$$

$$(7) \quad I_{46} = \frac{V_{BE} - V_{CODE}}{R_4 + R_6}$$

(8) $\beta I_B \approx I_C$

where $V_{BE} = -0.5V$

$V_{CODE} = -4.5V$

$I_C = 20$ ma

β min. $= 40$

Solution of (5) to (8) gives,

(9) $6.5(R_4 + R_6) - 4.0R_5 + 0.5R_5(R_4 + R_6) = 0$

Solving equations (4) and (9), and letting R_4 equal 3.3K, the values for R_5 and R_6 were found to be 26.2K and 2.72K ohms respectively.

Nominal values chosen for gate resistors are:

$R_4 = 3.3K$

$R_5 = 27K$

$R_6 = 2.7K$

Reset Gate Design

State	Code	Clock	Control	State of T_4
(1)	0	0	0	cutoff
(2)	0	0	1	cutoff
(3)	0	1	0	saturated
(4)	0	1	1	cutoff
(5)	1	0	0	cutoff
(6)	1	0	1	cutoff
(7)	1	1	0	cutoff
(8)	1	1	1	cutoff

TABLE 2

If states (3), (4) and (7), Table 2, are considered the gate will operate satisfactorily for all other states. Although logic input voltage levels are to be minus five volts, it will be assumed that a four and one half volt code pulse must be able to prevent a five and one half volt pulse from saturating transistor T_4. R_{10} was chosen as 1K therefore giving 6 milliamperes of collector current.

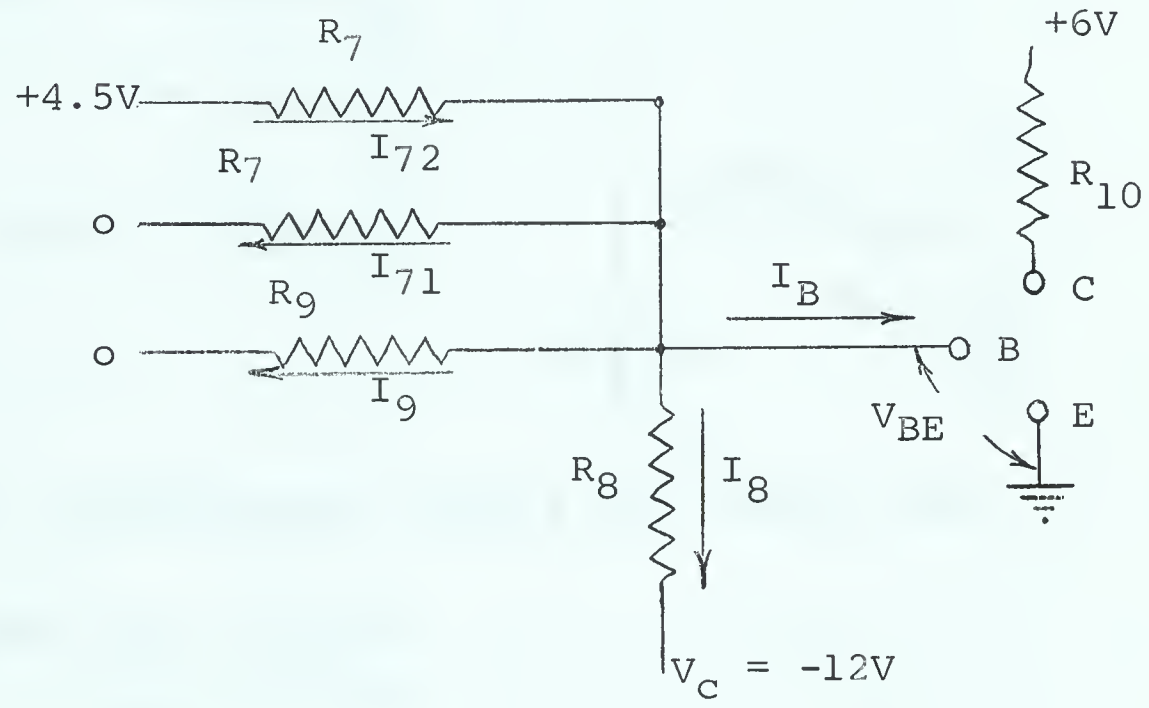


FIG. 14 EQUIVALENT CIRCUIT FOR INHIBIT GATE

Let $R_x = R_7 // R_9$

$I_x = I_{71} + I_9$

$V_{BE} = 0.5V$

$I_B = 0.4$ ma

From Fig. 14 the following equations are derived for state (3).

(1) $I_x + I_8 + I_B = I_{72}$

(2) $I_x = \frac{0.5}{R_x}$

$$(3)\quad I_{72} = \frac{V_{CLOCK} - V_{BE}}{R_7} = \frac{4.0}{R_7}$$

$$(4)\quad I_8 = \frac{V_{BE} - V_C}{R_8} = \frac{12.5}{R_8}$$

The circuit conditions for state (4) are shown in Fig. 15, from which equations (5) through (9) are obtained.

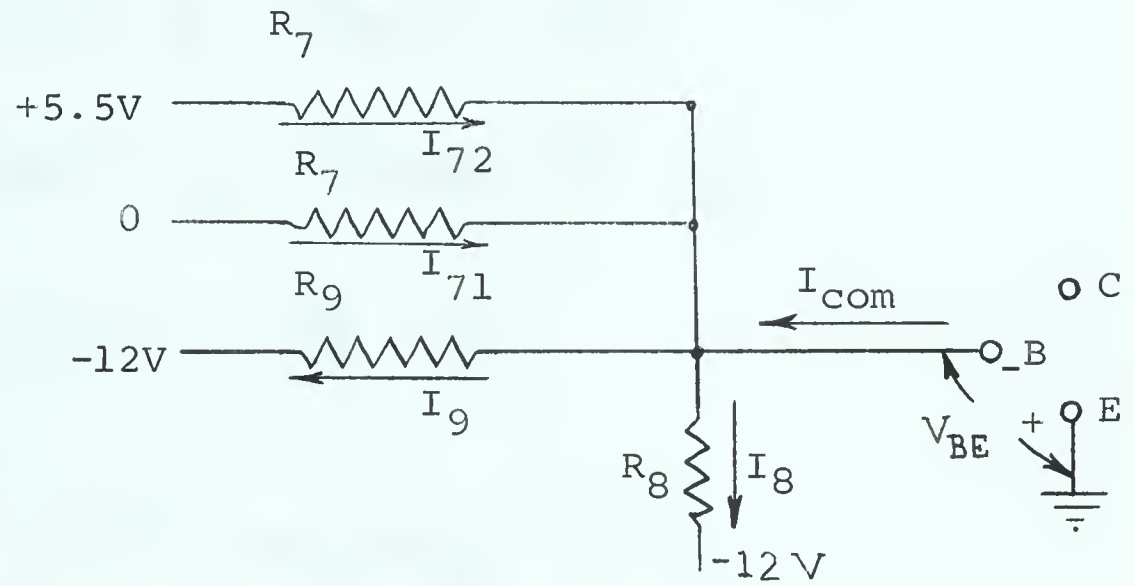


FIG. 15 EQUIVALENT CIRCUIT FOR INHIBIT GATE

where $I_{com} = 100\,\mu a$

$V_{BE} = -0.2V$

$$(5)\quad I_{71} + I_{72} + I_{com} = I_8 + I_9$$

$$(6)\quad I_{71} = \frac{V_{BE}}{R_7} = \frac{0.2}{R_7}$$

$$(7)\quad I_{72} = \frac{V_{CLOCK} - V_{BE}}{R_7} = \frac{5.7}{R_7}$$

$$(8)\quad I_9 = \frac{V_{CON} - V_{BE}}{R_8} = \frac{11.8}{R_8}$$

$$(9)\quad I_8 = \frac{V_C - V_{BE}}{R_9} = \frac{11.8}{R_9}$$

Equations (10) through (14) are obtained from Fig. 16 representing state (7).

$$(10)\quad I_{71} + I_8 = I_{com} + I_{72} + I_9$$

$$(11)\quad I_{71} = \frac{V_{BE} - V_{CODE}}{R_7} = \frac{4.3}{R_7}$$

$$(12)\quad I_8 = \frac{V_{BE} - V_C}{R_8} = \frac{11.8}{R_8}$$

$$(13)\quad I_{72} = \frac{V_{CLOCK} - V_{BE}}{R_7} = \frac{5.7}{R_7}$$

$$(14)\quad I_9 = \frac{V_{BE}}{R_9} = \frac{0.2}{R_9}$$

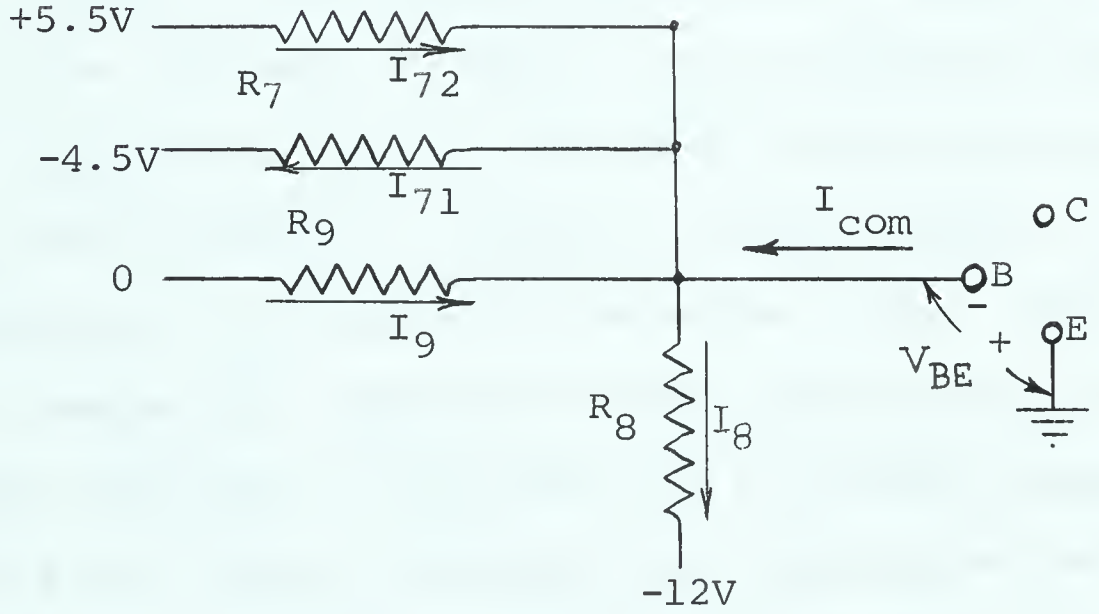


FIG. 16 EQUIVALENT CIRCUIT FOR INHIBIT GATE

where $I_{com} = 100\,\mu a$

$V_{BE} = -0.2V$

Solution of the preceeding equations gives the value of R_7, R_8 and R_9 as 3.3K, 21K and 9.2K ohms respectively.

Nominal values chosen are;

R_7 = 3.3K

R_8 = 18K

R_9 = 10K

R_{10} and C_3 values were obtained experimentally along with cross coupling capacitors to give as nearly equal turn-on and turn-off time as possible.

Reference Voltage Stability

The accuracy of the weighting network output will depend in part on the stability of the two reference voltages. The matching of collector-emitter saturation voltage and the forward voltage of the clamp diodes do not effect the stability of the reference voltage; only its absolute accuracy. However, V_{CE} saturation is a function of collector current and the diode voltage is related to diode current. Both of these voltages are temperature dependent also. Collector current changes are expected to vary approximately five per cent from flip-flop to flip-flop and a possible change of 0.1 millivolts per degree centigrade for temperature variations was measured. For normal room temperatures these differences in voltage can be ignored. Changes in clamp current in the diodes has been considered in the flip-flop design, but temperature variations which are approximately minus two millivolts per degree centigrade were not. The circuits of Fig. 17 will provide temperature compensation, but the change in output voltage is larger than in the uncompensated flip-flop

for equivalent load variations as the output voltage is now coupled to the reference supply through two diodes instead of one.

To temperature compensate, a diode D_0 whose characteristics are matched with D_1 and a resistor R_0 is added (Fig. 17). R_0 provides a forward bias for D_0 and can be a value which gives approximately the same current through D_1 and D_0. Adjustment of R_0 can also set the desired level of e_o within a small voltage range. Provision will be made on the printed circuit boards for these additional components but the components will not be included in the original construction. For the expected temperature variations of ten degrees centigrade a maximum error of 0.2 per cent will result because of the increased temperature if the diode voltage changes by approximately 2 millivolts per degree centigrade. This was considered satisfactory for the system at the present time.

If component temperature coefficients are the same, changes in reference voltages due to temperature variations will not alter the binary relationship but only the absolute accuracy.

The preceeding discussion does not consider variations in the twelve volt reference supply, but it is quite apparent that any noise or voltage variations will be transmitted to the weighting network output as error.

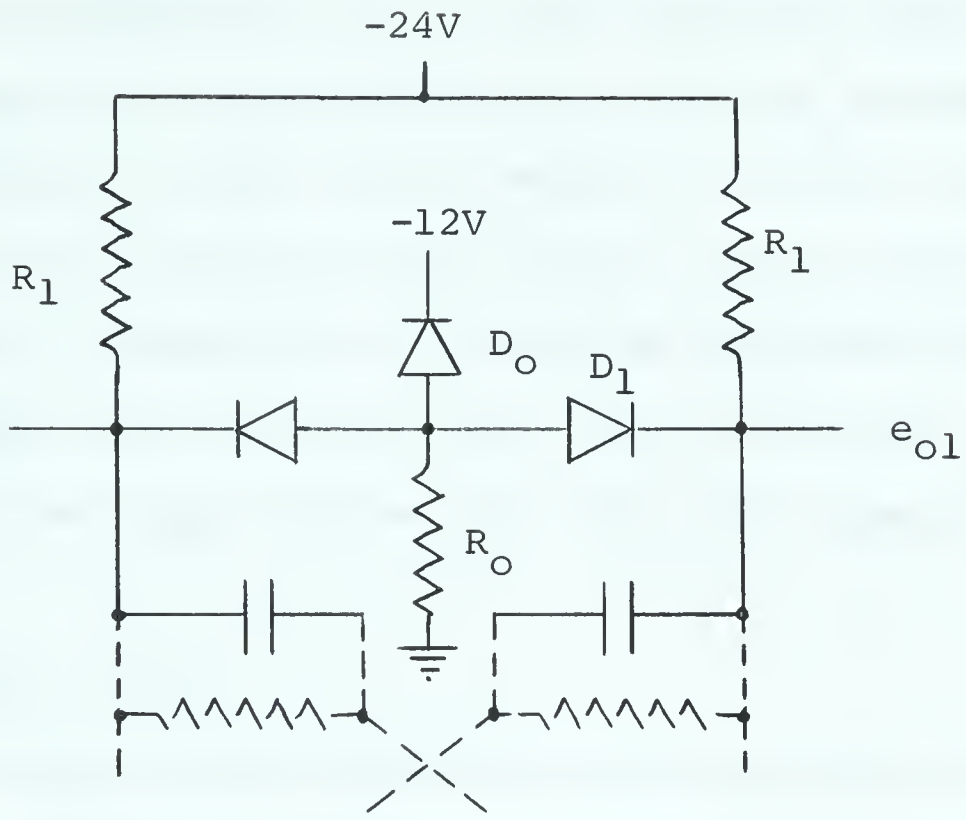


FIG. 17 TEMPERATURE COMPENSATION FOR CLAMPED FLIP-FLOPS

Binary Weighted Network

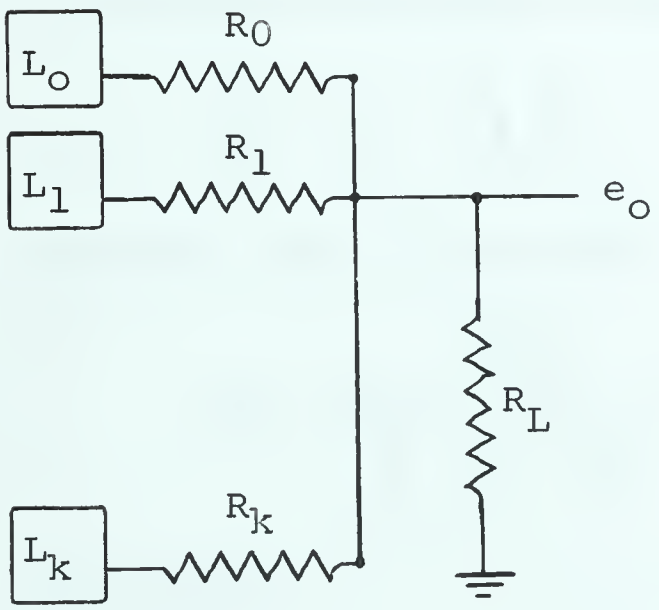


FIG. 18

BINARY WEIGHTED NETWORK

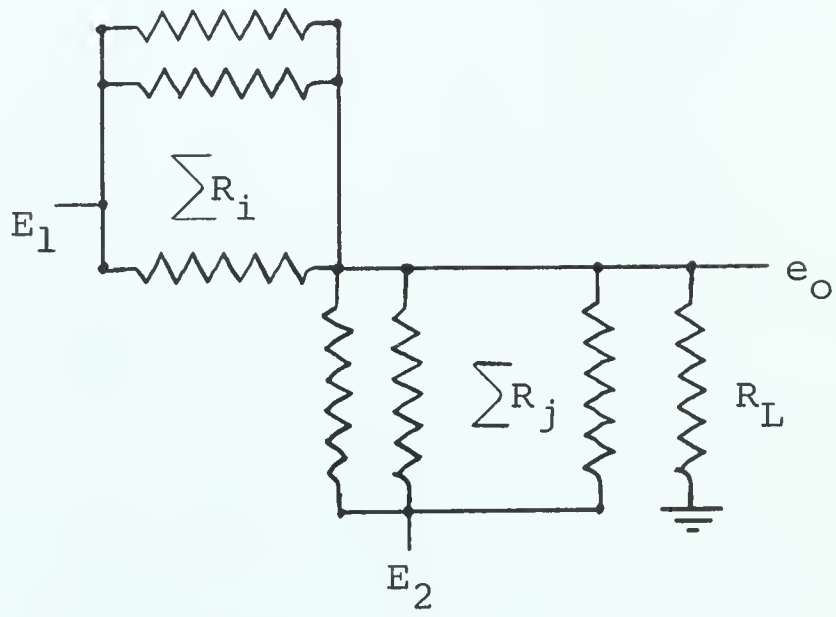


FIG. 19

EQUIVALENT CIRCUIT FOR BINARY WEIGHTED NETWORK

Depending on the position of L_k, the flip-flop output, either reference E_1 or E_2 is applied to the weighting network. The equivalent circuit of Fig. 18 is shown in Fig. 19, where R_i are the resistors connected to E_1 and R_j are the resistors connected to E_2. Susskind(2) derives an expression for output voltage and will be shown below for convenience. Considering ideal voltage sources and using the superposition theorem,

$$e_o = E_{01} + E_{02}$$

where E_{01} and E_{02} is the output voltage due to E_1 and E_2 respectively. Replacing E_2 by a short circuit,

$$(1) \quad E_{01} = \frac{\frac{1}{\sum \frac{1}{R_j} + \frac{1}{R_L}}}{\frac{1}{\sum \frac{1}{R_j} + \frac{1}{R_L}} + \frac{1}{\sum \frac{1}{R_i}}} E_1$$

Rearranging the above terms and letting

$$\frac{1}{R_i} + \frac{1}{R_j} = \sum_{o}^{n} \frac{1}{R_k}$$

equation (2) is obtained.

$$E_{01} = \frac{\sum \frac{1}{R_i}}{\sum_{o}^{n} \frac{1}{R_k} + \frac{1}{R_L}} E_1$$

Similarly,

$$(3) \quad E_{02} = \frac{\sum \frac{1}{R_j}}{\sum_{o}^{n} \frac{1}{R_k} + \frac{1}{R_L}} E_2$$

Combining equations (2) and (3)

$$(4)\quad e_o = \frac{1}{\sum_{o}^{n} \frac{1}{R_k} + \frac{1}{R_L}} \left[E_1 \sum \frac{1}{R_i} + E_2 \sum \frac{1}{R_j} \right]$$

For a binary weighted network the value of any resistor is

$$R_k = \frac{R}{2^k}$$

where R is the value of the largest resistor. Hence

$$(5)\quad \sum_{o}^{n} \frac{1}{R_k} = \sum_{o}^{n} \frac{2^k}{R} = \frac{1}{R} \left[2^{n+1} - 1 \right]$$

Also

$$(6)\quad \sum \frac{1}{R_j} = \sum \frac{2^j}{R} = \frac{1}{R} P$$

where P is the value of the number to be decoded.

Since,

$$\sum \frac{1}{R_j} + \sum \frac{1}{R_i} = \sum_{o}^{n} \frac{1}{R_k}$$

then

$$\sum 2^j + \sum 2^i - 2^{n+1} - 1$$

and

$$\sum 2^i = 2^{n+1} - 1 - P$$

therefore

$$\sum \frac{1}{R_j} = \frac{1}{R} \sum 2^i = \frac{1}{R} \left[2^{n+1} - 1 - P \right]$$

Substitution of (5), (6) and (7) into equation (4) gives,

$$e_o = \frac{1}{\frac{1}{R_L} + \frac{2^{n+1} - 1}{R}} \left[\frac{E_1}{R} (2^{n+1} - 1 - P) + \frac{E_2}{R} P \right]$$

$$(8) \quad e_o = \frac{1}{\frac{R}{R_L} + 2^{n+1} - 1} \left[E_1(2^{n+1} - 1) + P(E_2 - E_1) \right]$$

Therefore the output is a linear function of P. The change in output voltage per change in number is,

$$(9) \quad \frac{\Delta e}{\Delta P} = \frac{E_1 - E_2}{\frac{R}{R_L} + 2^{n+1} - 1}$$

and is only dependent on the accuracy of the resistors and the constancy of the reference voltages, if R_L remains constant.

To provide accurate resistance values, one per cent resistors and a series trimming potentiometer will be used. To ensure uniform resistance values over the working temperature range, the temperature coefficient must be small.

Corning, Type N70 resistors meets the required specifications for this project. Fifteen turn Bourns wire wound potentiometers were chosen for setting the network resistors to required value. A compromise must be made when specifying the values of the divider network resistors. The largest resistor must have sufficient current to be detectable above the noise level and the smallest resistor current must not produce any significant change in the reference voltage. These changes can become significant for the larger bits when diode clamping is used for the reference voltage. If the output of the weighting network is at virtual ground as is

the case when an operational amplifier is used, the current in each resistor is independent of the state of the other bits. If this is not so the current in each resistor is a function of the other bits being "zero" or "one". To stay within practical limits for R_L and network resistors and still maintain fairly constant current in the most significant bits as the output changes through all incremental values, a choice of 1.5K for R_L and 3K for R_n was made. This requires the value of the largest resistor to be 1.6 megohms. Although such a large value is not desirable, satisfactory operation of the weighting network is expected.

With the most significant bit in the one state and all other bits "zero" the output voltage given by equation (8) is

$$e_o = 3.07 \text{ volts}$$

For all bits being "one" the output voltage now is 6.15 volts. The change in current in the smallest weighting network resistor is equal to the differences of the above voltages divided by the resistor value. The maximum change in current expected is then 1 ma. Maximum current changes in other resistors and therefore in the flip-flop clamp diodes will be less in proportion to the resistance values.

Inverting Amplifier

A negative input voltage from the weighting network can be converted to a positive or negative output voltage, depending on the information carried by the sign bit, with the circuit shown in Fig. 20. Transistors T_1 and T_2 comprise

part of the differential amplifier with T_3 as its constant current source. To direct the input signal into the base of T_1 or T_2 identical gates are employed with T_4 and T_5 as a portion of one gate and T_6 and T_7 as the other. These gates are controlled by the plus-minus flip-flop.

If a negative output voltage is required transistor T_5 is kept cutoff allowing T_4 to act as an emitter follower. This lets the input signal appear at the base of T_1 and hence at the collector of T_2 non-inverted. Meanwhile transistor T_6 is cutoff and T_7 saturated therefore applying a constant potential, set by T_8, to the base of T_2.

For positive output voltages the roles of the gates are interchanged. This allows the negative input signal to drive the base of T_2 giving a positive output voltage at its collector.

One of the major problems in the design of this amplifier is to stabilize the gain for large signal inputs and minimize drift which is always inherent in D.C. amplifiers.

The inverting amplifier in Fig. 20 has been reduced to the differential stage plus two signal generators e_1 and e_2 and their equivalent source impedances (Fig. 21). This circuit provides a more convenient starting point for the analysis of gain and drift stabilization.

If T_1 and T_2 are assumed identical for purposes of analysis, although they cannot be in reality, an insight into the operating characteristics of the differential amplifier

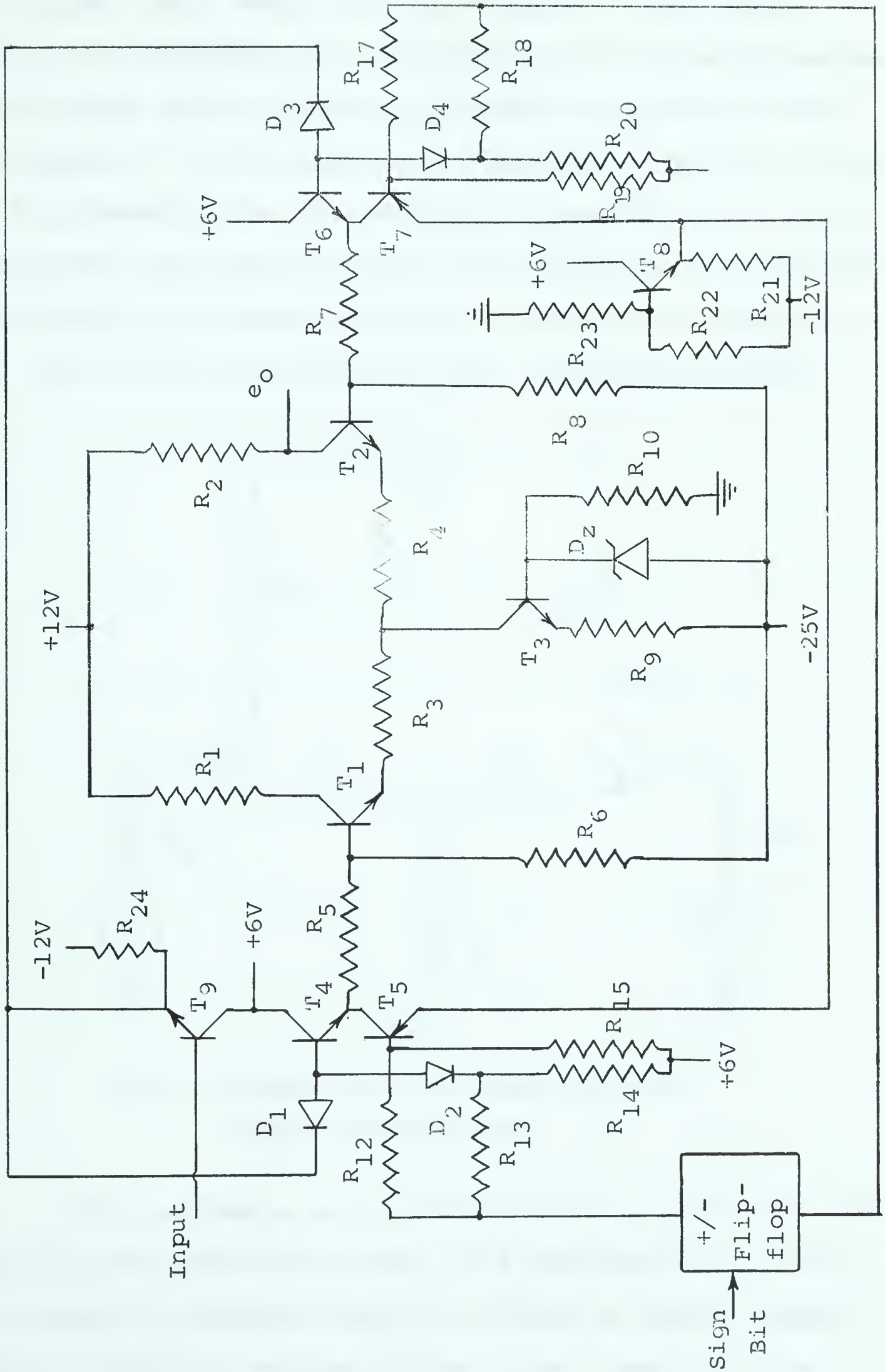


FIG. 20 INVERTING AMPLIFIER

as a large signal device can be obtained. Using hybrid parameters and accounting for variations in these parameters due to large signal operation provides a convenient means for analysis. In the ideal case where small signals are used the h- parameters can be considered linear for small excursions about the operating point and because of the differential circuit the changes in T_1 are cancelled by changes in T_2. Such is not the case for large signal applications.

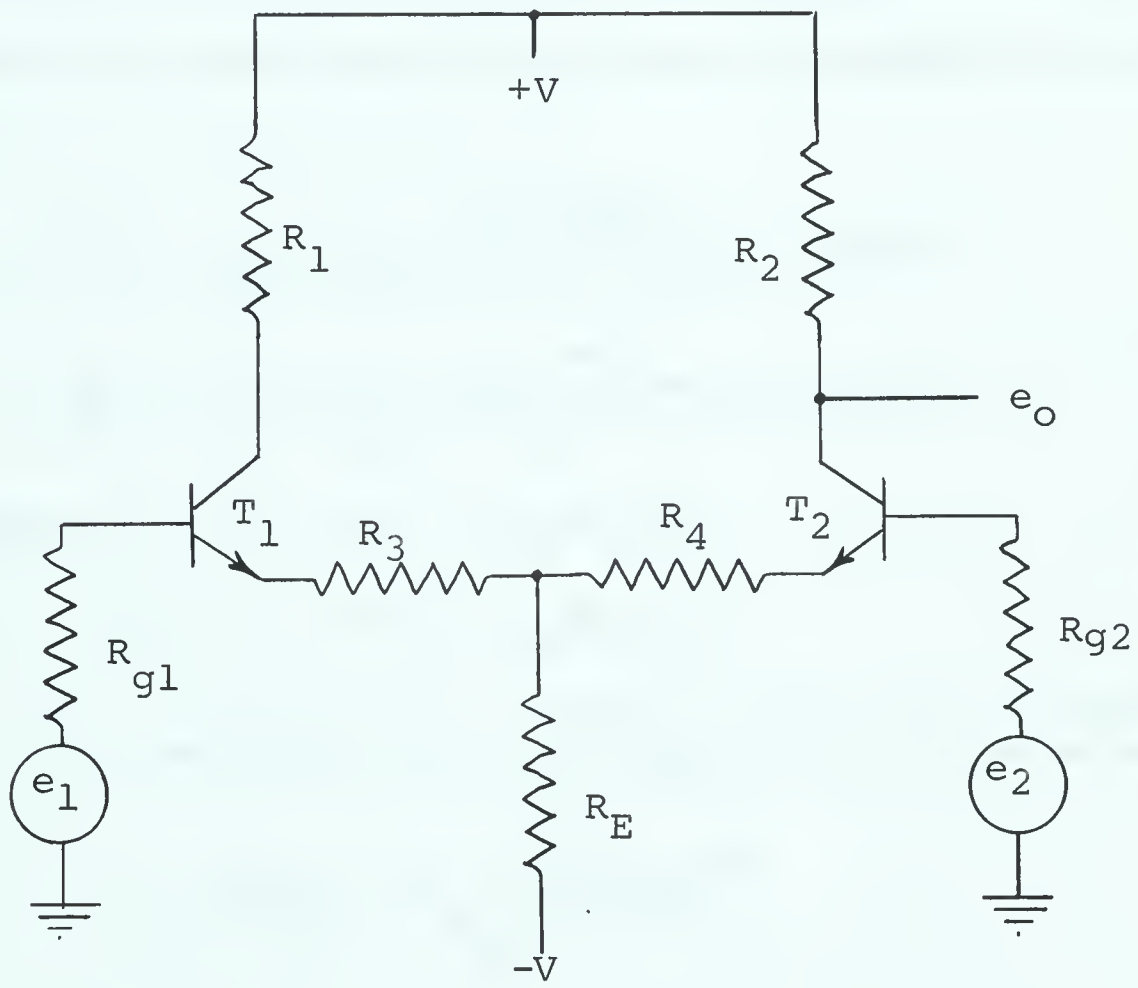


FIG. 21 SIMPLIFIED REPRESENTATION OF INVERTING AMPLIFIER

Drift becomes a major problem in D.C. amplifiers and again with matched transistors, in a differential circuit, any change in parameters due to a change in ambient temperature is cancelled because of the circuit configuration.

In a large signal device the temperature of the transistors is not only a function of ambient conditions but also related to the magnitude of the output signals, since for large changes in collector voltage the power dissipated does vary appreciably. If this causes a temperature difference to exist between T_1 and T_2 the transistor characteristics can no longer be considered matched and drift results.

The common base hybrid parameters are convenient for obtaining the differential amplifier characteristics. Slaughter(4) has derived the following expression for voltage gain.

$$(1) \quad A_{12} = \frac{e_o}{e_1} = \frac{+ \alpha_2 R_2}{r_{h1} + r_{h2} + R_3 + R_4 + A + B + C}$$

$$(2) \quad A_{22} = \frac{e_o}{e_2} = \frac{- \alpha_2 R_2}{r_{h1} + r_{h2} + R_3 + R_4 + A + B + D}$$

where $A = (1 - \alpha_1 + Y_{C1} R_1) R_{g1}$

$B = (1 - \alpha_2 + Y_{C2} R_2) R_{g2}$

$$C = \frac{(r_{h1} + (1 - \alpha_1) R_{g1})\ (r_{h2} + (1 - \alpha_2) R_{g2})}{R_E}$$

$$D = \frac{(r_{h1} + (1 - \alpha_1) R_{g1})^2}{R_E}$$

$r_{h1} = h_{ib}$

$\alpha = -h_{fb}$

$Y_c = h_{ob}$

R_E is the resistance seen looking into the collector of T_3 and subscripts 1 and 2 refer to transistors T_1 and T_2

respectively. With a constant current source such as T_3 the value of R_E is sufficiently large so that terms C and D may be ignored. This will be verified later. This leaves identical gain expressions except for the minus sign in A_{22}. The major source of difficulty now remaining are the terms r_h, α, and Y_c. These parameters are not constant but depend on the operating point and therefore variations can be expected for large signal operation. If R_3 and R_4 can be made much larger than terms A and B then gain is no longer a function of Y_c and α in these two terms. The gain expression may now be approximated by:

$$(3)\quad |A_{22}| = |A_{12}| = \frac{\alpha_2 R_2}{r_{h1} + r_{h2} + R_3 + R_4}$$

If the variations in r_{h1} and r_{h2} can be swamped by emitter resistors R_3 and R_4 then only one transistor parameter remains which might cause trouble for large signal operation. This is the term α in the numerator. An example will show the significance of variations in this parameter. If the common-emitter current gain of a transistor is 100, a 10 per cent increase in this value would change α by 0.09 per cent. If the transistor current gain was 150, a 10 per cent increase in this value would result in a 0.07% increase in α. Under large signal conditions the α term in the numerator should pose no problem as the measured α changes by less than this amount. Best results are obtained for transistors with a large current gain.

The next thing to consider is the value of R_3 and R_4 which will swamp the changes in r_{h1} and r_{h2}. Fig. 22 is a plot of h_{ib} versus emitter current for a typical 2N929 transistor. As can be seen, h_{ib} is quite dependent on the operating point and for large signals its variation can be considerable.

If two transistors with identical h_{ib} are used in a differential stage the change in $r_{h1} + r_{h2}$ is much less than h_{ib} for a single transistor since an increase in emitter current in one transistor corresponds to an almost identical decrease in emitter current in the second transistor. The change in $r_{h1} + r_{h2}$ is shown in Fig. 23 for large excursions about various operating points. The advantage of using a differential amplifier is quite apparent. Also an estimate of the value of R_3 and R_4 can be obtained to give desired gain linearity for a chosen quiescent point.

This amplifier must be direct coupled, therefore stability of the operating point must be considered. Low collector currents, common heat sinking of T_1 and T_2 and matched V_{BE} temperature coefficients will help reduce transistor unbalance. As stated earlier the junction temperature of the transistor will vary appreciably because of large changes in power disipation when used as a large signal device.

Leakage current can be ignored if low leakage silicon transistors are used and the temperature dependency of the h-parameters can be considered when choosing component values

to give good gain stability.

The 2N929 transistor was chosen for the differential stage with the collector current set at 1.2 ma. For a quiescent output of zero volts,

$$R_1 = R_2 = \frac{V_{CC}}{I_C} = 10K \text{ ohms}$$

The constant current source must supply approximately 2.4 ma of current therefore,

$$R_9 = \frac{V_Z - V_{BE_3}}{2I_C} = 2.96K \text{ ohms.}$$

The voltage gain of the differential amplifier is not too important as another amplifier will follow to provide a lower output impedance. If a collector swing of plus and minus five volts is assumed the value of the h- parameters can be found.

$$h_{ib_{min}} = 50 \text{ ohms} = r_{h1} + r_{h2}$$

$$h_{ib_{max}} = 70 \text{ ohms} = r_{h1} + r_{h2}$$

$$\Delta h_{ib_{max}} = 20 \text{ ohms}$$

$$h_{fb_{min}} = 0.99$$

$$h_{ob_{max}} = 0.5 \times 10^{-6} \text{ ohms}$$

$$h_{ob_{min}} = 2.0 \times 10^{-8} \text{ ohms}$$

$$h_{rb} = 6 \times 10^{-4}$$

Evaluating D in Egn. 2 gives a value of less than 0.01 where,

$$R_E = \frac{h_{ib} + R_9 + R_5(1 + h_{fb})}{h_{ob}(h_{ib} + R_9 + R_5) - h_{fb}h_{rb}}$$

$$\geq 1 \text{ megohm}$$

$$R_5 = 1K \text{ ohms}$$

$$R_{g1} = R_{g2} = 5K \text{ ohms maximum}$$

Terms C and D can be ignored. The values for A and B are less than 50 ohms for R_g = 5K with the change over the operating range less than 10 ohms. To swamp the variations in $r_{h1} + r_{h2}$ the value of R_3 and R_4 was chosen as 2.7K. The gain of the differential amplifier will be approximately,

$$A_v = \frac{2R_2}{r_{h1} + r_{h2} + R_3 + R_4} = 1.8$$

The input impedance of the following stage must be specified before bias conditions are evaluated for transistors T_1 and T_2 so that approximately equal positive and negative outputs can be obtained. If this input impedance is 20K ohms the Thevenin equivalent collector resistor for T_1 and T_2 is 6.6K ohms and the Thevenin voltage is 8 volts. For a quiescent output of zero volts the base of T_1 and T_2 was biased to -8 volts.

Referring to Fig.20, the source resistance R_{g1} and R_{g2} is $\frac{(R_5 + R_{OF})R_6}{R_5 + R_6 + R_{OF}}$ for identical switches where R_{OF} is the output impedance of follower T_4.

Assume $R_{OF} = h_{ib} = 30$ ohms

Also $\frac{R_5 V_B}{R_5 + R_6} = -8$ volts

Solving the above equations for R_{g1} = 3K ohms gives

the nominal values of R_5 and R_6 as

$$R_5 = 4.7K$$

$$R_6 = 10K$$

Assuming follower circuits have unity gain, the total voltage gain of the inverting amplifier is

$$A_v = \frac{R_6}{R_5 + R_6} \quad A_{22}$$ where A_{22} is given in equation 3.

The calculated value is 0.83.

The effect of input follower T_9, D_1 and D_3 must still be considered. The gain of an emitter follower can be expressed as(5),

$$A_v = \frac{R_L}{h_{ib} + R_L}$$

The change in the voltage drop across diodes D_1 and D_3 for a negative input voltage will tend to cancel the changes in h_{ib} if the diode current is properly chosen. Since h_{ib} and the forward diode voltage is non-linear it is rather difficult to obtain a meaningful analysis therefore the diode current was found experimentally.

The temperature drift of the amplifier and the switches is primarily due to changes in V_{BE} and the forward voltage drop across diodes D_1 and D_3. The zero input signal at the emitter of T_4 or T_6 is

$$V_i = V_{CEF_{sat}} + V_{BE_9} + V_{D_1} = V_{BE_4}$$

where $V_{CEF_{sat}} = V_{CE_{sat}}$ of the flip-flops.

For equal input signals to the differential amplifier from

both switches, diodes D_1 and D_3 must be matched. V_{BE_4} and V_{BE_6} must also be the same value. The reference voltage at the differential transistor not receiving the input signal is

$$V_r = V_{CE5_{sat}} + V_{BE_8} \text{ when } R_{23} \text{ is zero.}$$

The saturation voltage of T_5 and T_7 must therefore be matched to have identical reference voltages for both switches.

Potentiometer R_{23} corrects the reference potential for small differences in V_i and V_r. The temperature coefficients of D_1 and D_3 are the same as V_{BE_4} and V_{BE_5} and therefore cancel since the voltage drop across the diodes is of the opposite polarity as V_{BE}. If transistors T_5 and T_7 are 2N1309, the same as the flip-flop transistors, and T_8 and T_9 are matched transistors then drift in the switches and input emitter follower will be minimized.

Gate Design

The equations for T_5 cutoff can be obtained from Fig. 24(a).

$$(4) \quad \frac{V_D - V_{BE} + 0.6}{R_{15}} - \frac{V_{BE} - 0.6}{R_{13}} = I_{com}$$

Saturation conditions for T_5 are given in Fig. 24(b) from which the following equations are obtained.

$$(5) \quad \frac{V_{BE} - 0.6 - V_S}{R_{13}} = \frac{V_D - V_{BE} + 0.6}{R_{15}} + I_b$$

$$(6) \quad \beta I_B \approx I_c$$

Solution of equations (4) to (6) gives nominal values of R_{12} and R_{14} as 18K and 82K ohms respectively.

For D_2 non-conducting, the proper bias current for D_1 is supplied by making R_{11} equal to 33K ohms. With D_2 conducting the equivalent circuit is given in Fig. 25, from which the following equations are derived.

$$\frac{V_{cc} - V_f}{R_{11}} + \frac{V_D - V_y}{R_{14}} + \frac{V_s + V_y}{R_{12}} = 0$$

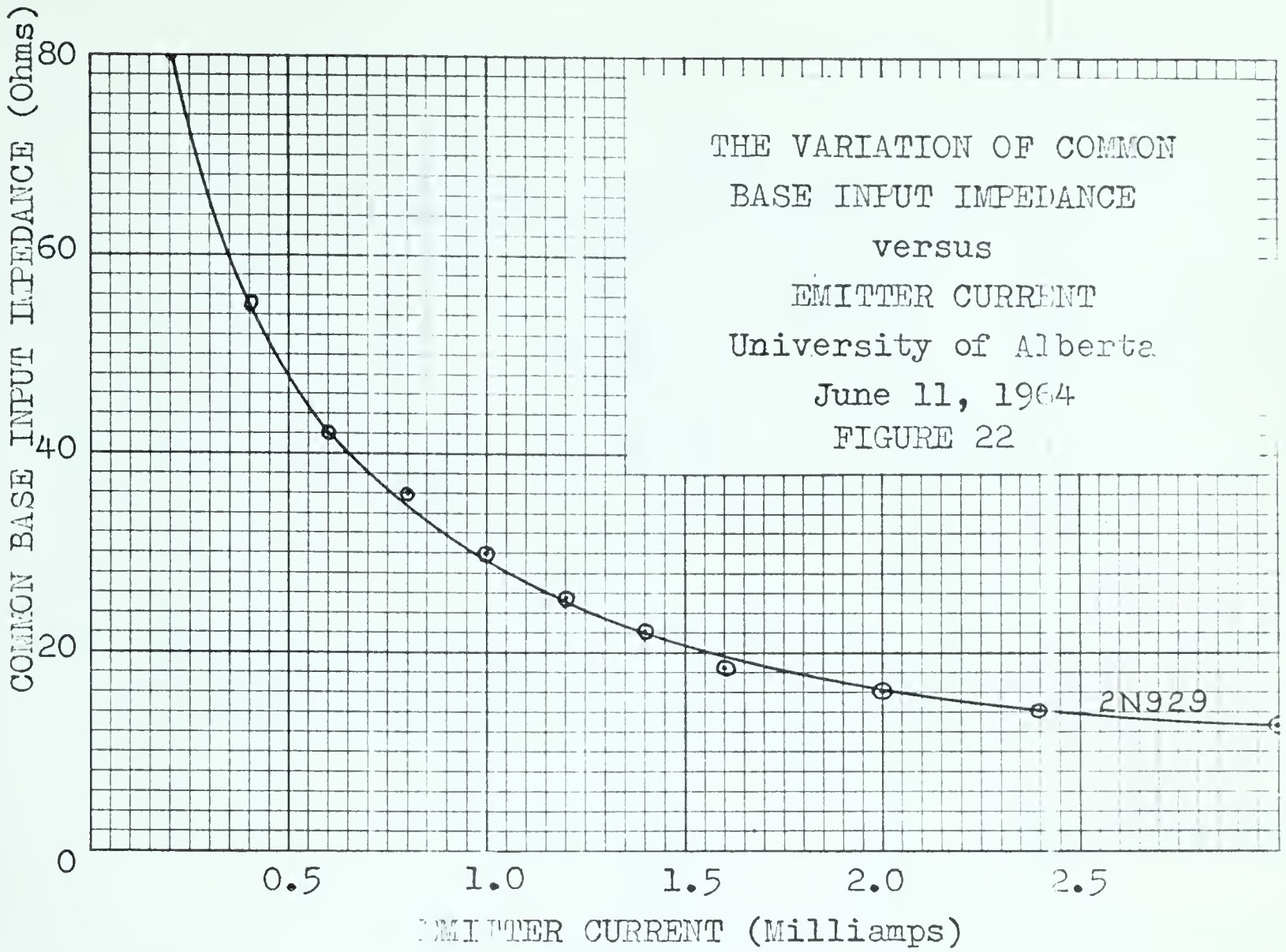
$$V_f = V_y + V_{D_2}$$

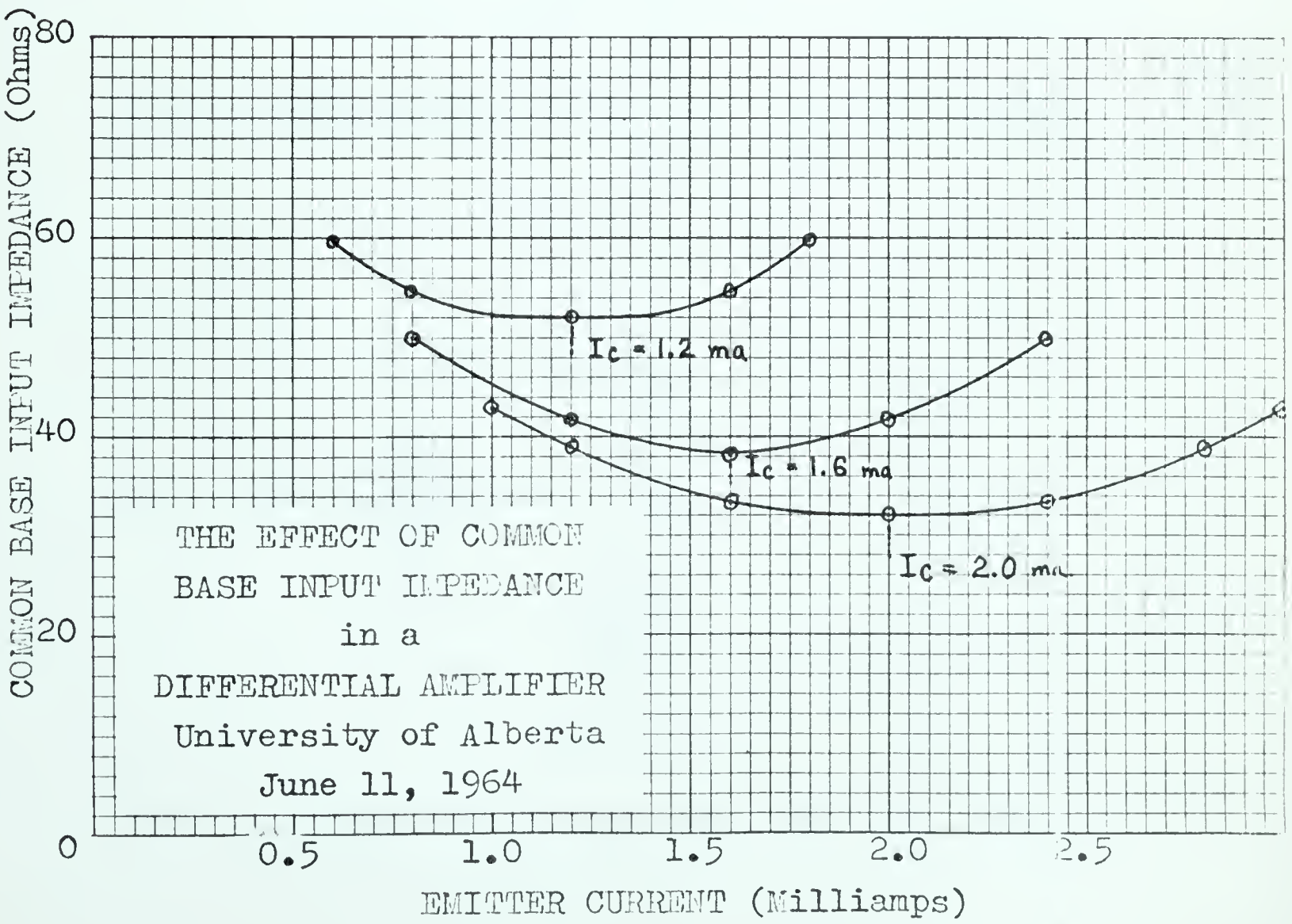
The equations are satisfied if R_{12} and R_{15} equal 15K and 47K respectively. The switch containing T_6, T_7, D_3 and D_4 will contain identical components. The emitter resistors R_{21} and R_{24} were 3.3K. Resistor R_{10} in the constant current supply must be selected to provide a zener temperature coefficient that will match the V_{BE} coefficient of T_3. Satisfactory adjustment of the reference voltage is obtained with potentiometer R_3 equal to 100 ohms and R_{22} at 33K ohms.

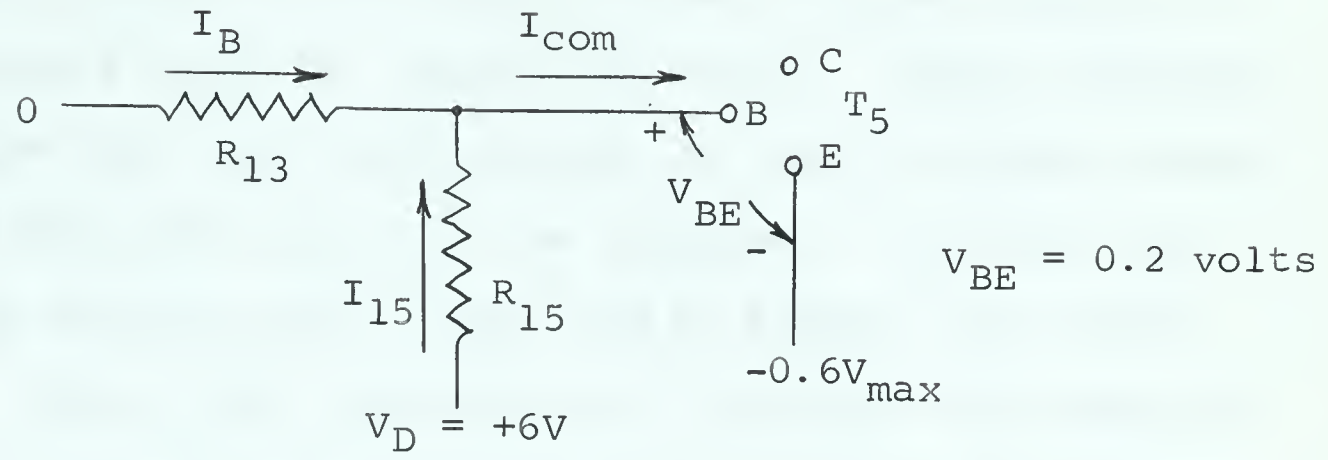
Output Amplifier

The circuit in Fig. 26 was chosen to provide a D.C. output stage with lower output impedance than the differential inverting amplifier. A second function of this amplifier is to provide a convenient means of gain adjustment for setting the decoder voltage output.

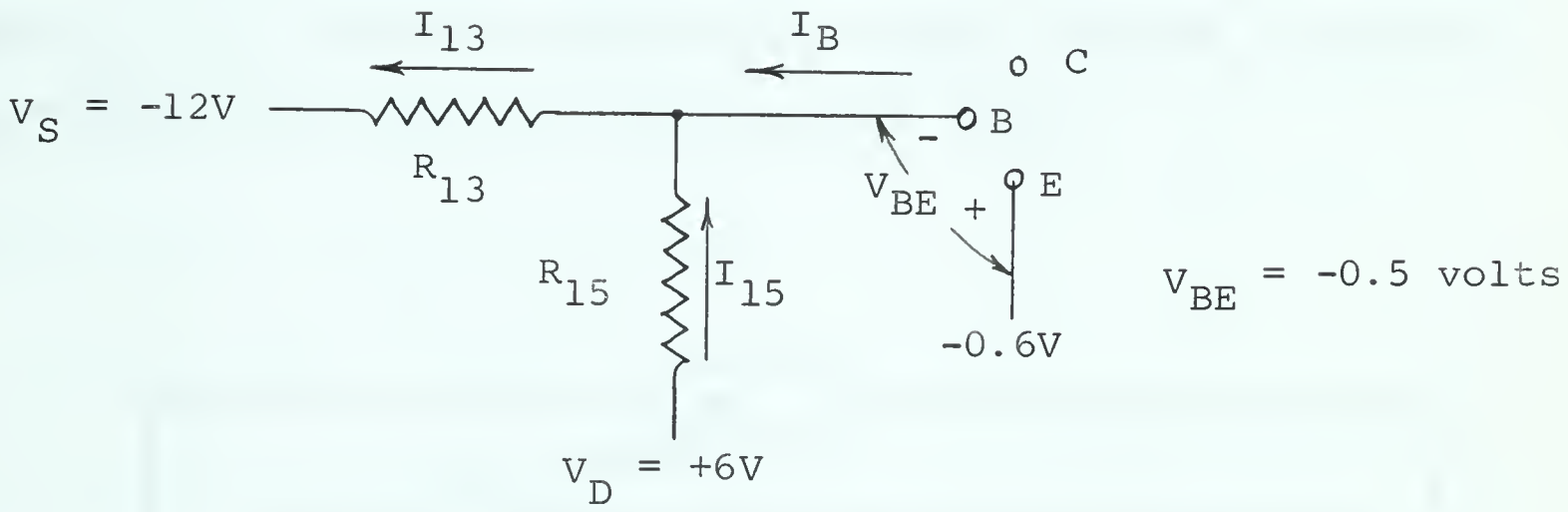
A differential input stage was used to minimize input drift, as drift in this stage is not reduced by feedback.


COMMON BASE INPUT IMPEDANCE (Ohms)
80
60
40
20
0
0.5
1.0
1.5
2.0
2.5
EMITTER CURRENT (Milliamps)
THE VARIATION OF COMMON
BASE INPUT IMPEDANCE
versus
EMITTER CURRENT
University of Alberta
June 11, 1964
FIGURE 22
2N929


COMMON BASE INPUT IMPEDANCE (Ohms)
80
60
40
20
0
0.5
1.0
1.5
2.0
2.5
EMITTER CURRENT (Milliamps)
THE EFFECT OF COMMON
BASE INPUT IMPEDANCE
in a
DIFFERENTIAL AMPLIFIER
University of Alberta
June 11, 1964
Ic = 1.2 ma
Ic = 1.6 ma
Ic = 2.0 ma



(a)



(b)

FIG. 24 EQUIVALENT CIRCUITS FOR AMPLIFIER GATES

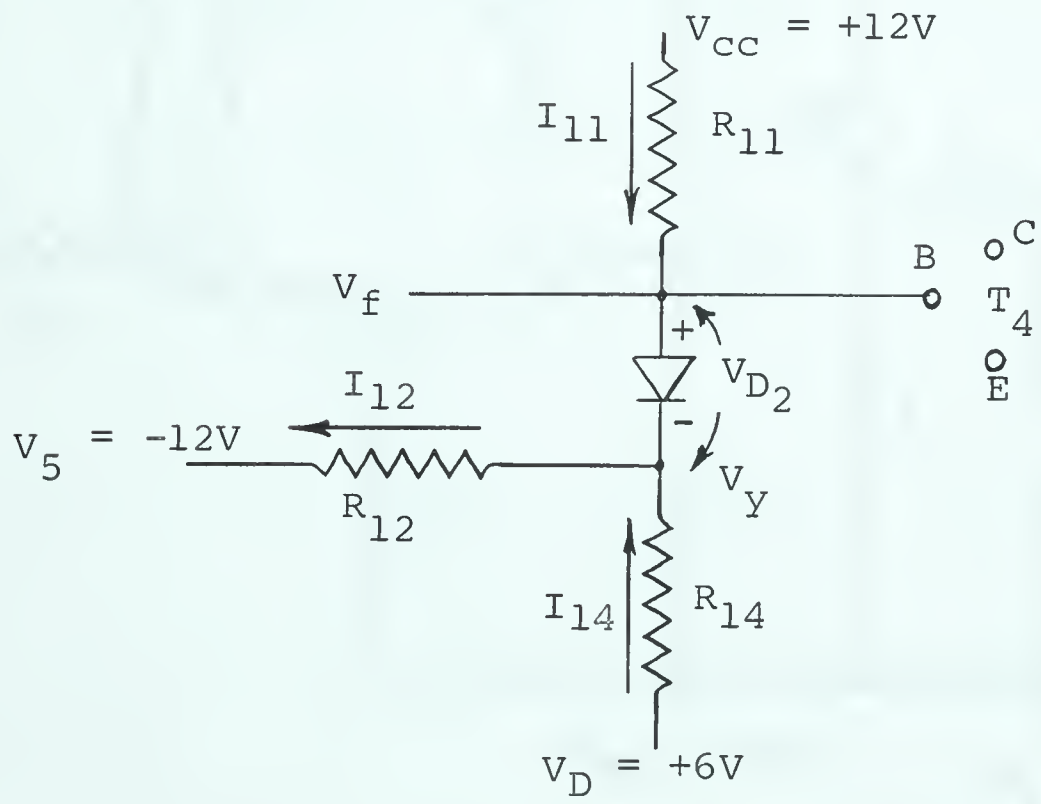


FIG. 25 EQUIVALENT CIRCUITS FOR AMPLIFIER GATES

Transistor T_3 used as an emitter follower reduces loading of the differential stage by resistor R_8 and R_9. These resistors set the proper bias for transistor T_4 so that a maximum output of plus and minus ten volts can be obtained. Transistor T_4 provides the second stage of gain and T_5 reduces the output impedance. Using a PNP transistor for T_5 allows the positive output swing to be greater than an equivalent NPN unit because the collector of T_4 is always negative with respect to the emitter of T_5 therefore allowing the output voltage to approach V_{cc} without distortion at the collector of T_4.

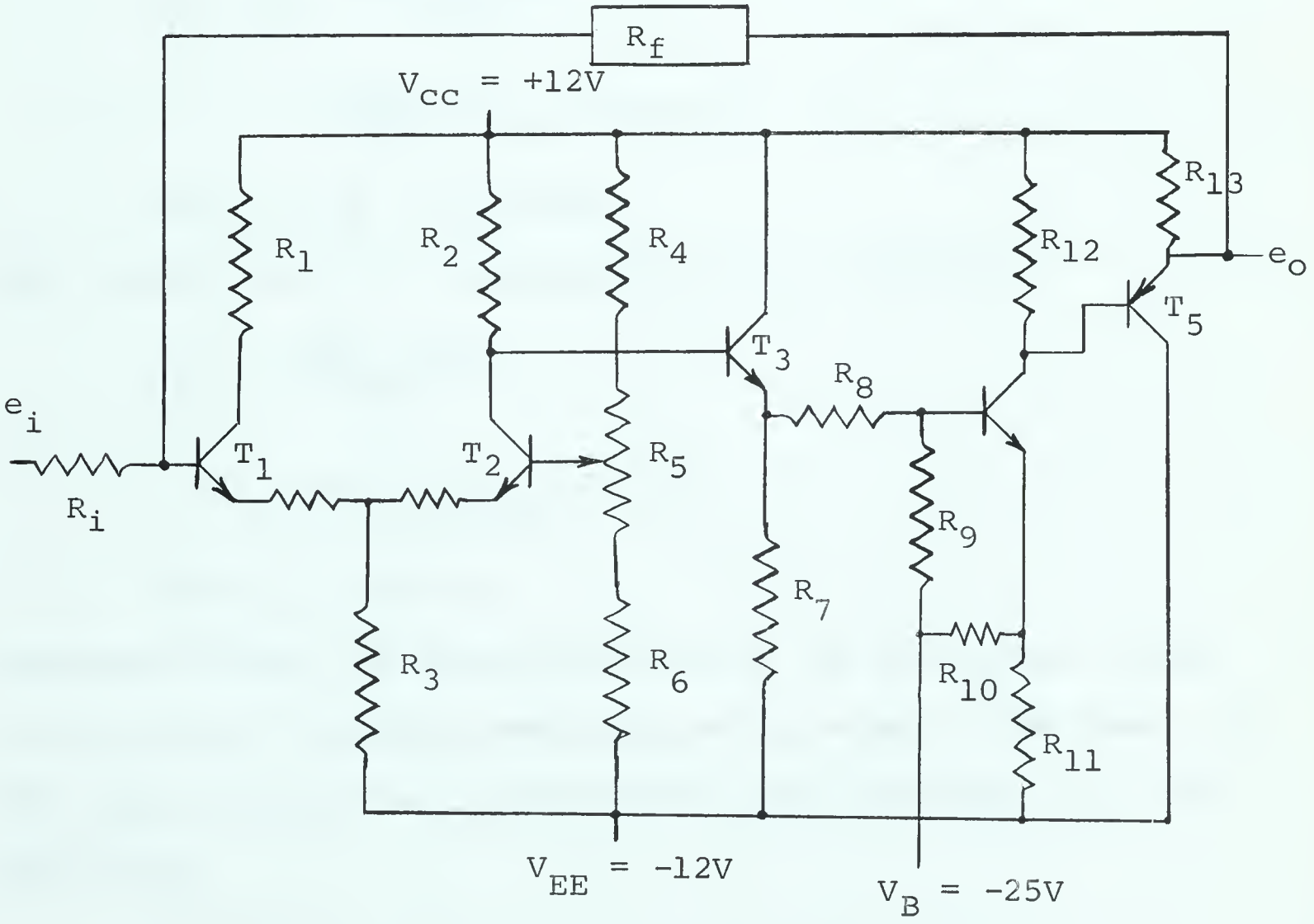


FIG. 26 OUTPUT AMPLIFIER

To minimize drift T_1 and T_2 should operate at low collector currents and be kept at the same temperature so that maximum drift cancellation will result for the two temperature sensitive base-emitter voltages. The low leakage current of silicon transistors make I_{CO} insignificant compared to the temperature sensitivity of V_{BE}. The 2N929 transistor was chosen for its low leakage (I_{CO} = .01μa at 25° C) and fairly high current gain at low collector currents. The operating point was set at a collector current of 170μa and a collector-emitter voltage of four volts. The value of R_1 and R_2 can now be calculated.

$$R_1 = R_2 = \frac{V_{CC} - V_{CE}}{I_C}$$

$$= \frac{12 - 4}{170 \times 10^{-6}} = 47.1K$$

Let $R_1 = R_2 = 47K$ ohms.

The current in R_3 is approximately $2I_C$, therefore:

$$R_3 = - \frac{V_{BE} + V_{EE}}{2I_C}$$

$$= \frac{12 - 0.6}{2 \times 170 \times 10^{-6}} = 33.6K$$

Let R_3 = 33K ohms.

Current through the bias resistors R_4, R_5 and R_6 was chosen to be 1.5 ma therefore making R_4 and R_6 equal to 8K ohms. A 100 ohm potentiometer R_5 provides a zero adjustment for the amplifier.

The voltage gain given by Slaughter(4) is:

$$A_v = \frac{\alpha_1 R_2}{h_{ib_1} + h_{ib_2} + (1 - \alpha_1 + h_{ob_1} R_1) R_{g1} + (1 - \alpha_2 + h_{ob_2} R_2) R_{g2} + D}$$

$$\text{where } D = \frac{(h_{ib_1} + (1 - \alpha_1) R_{g1})\ (h_{ib_2} + (1 - \alpha_2) R_{g2})}{R_3}$$

and $h_{ib} = 120$ ohms

$h_{ob} = 2.5 \times 10^{-8}$ ohms

$\alpha = -h_{fb} = 0.99$

The numerical subscripts refer to transistors T_1 and T_2. For a source resistance of 4K ohms for R_{g1}, and R_{g2} equal to 20K ohms, the calculated voltage gain is:

$$A_v = 95$$

Transistor T_3 used in the emitter-follower configuration reduces loading the differential amplifier. For practical purposes the input resistance looking in at the base of T_3 can be approximated by βR_L, where R_L is the appropriate combination of R_7, R_8, R_9 and the input impedance seen at the base of T_4. The input impedance of the emitter-follower was chosen to be at least 0.5 megohms. Using a T1495 for T_3 with a minimum current gain of 100, R_L must be no smaller than 5K ohms. To determine the value of R_7, R_8 and R_9 the operating point of T_4 must be set.

Neglecting emitter current of T_4 the values of R_{10} and R_{11} can be found. From Fig. 27 the equations are;

$$\frac{V_{EE} - V_B}{R_{10} + R_{11}} = I_{10}$$

$$\frac{R_{11}(V_{EE} - V_B)}{R_{10} + R_{11}} = V_{EE} - V_x$$

Therefore R_{10} = 367 ohms and R_{11} = 67 ohms.

Let R_{10} = 330 ohms

R_{11} = 68 ohms

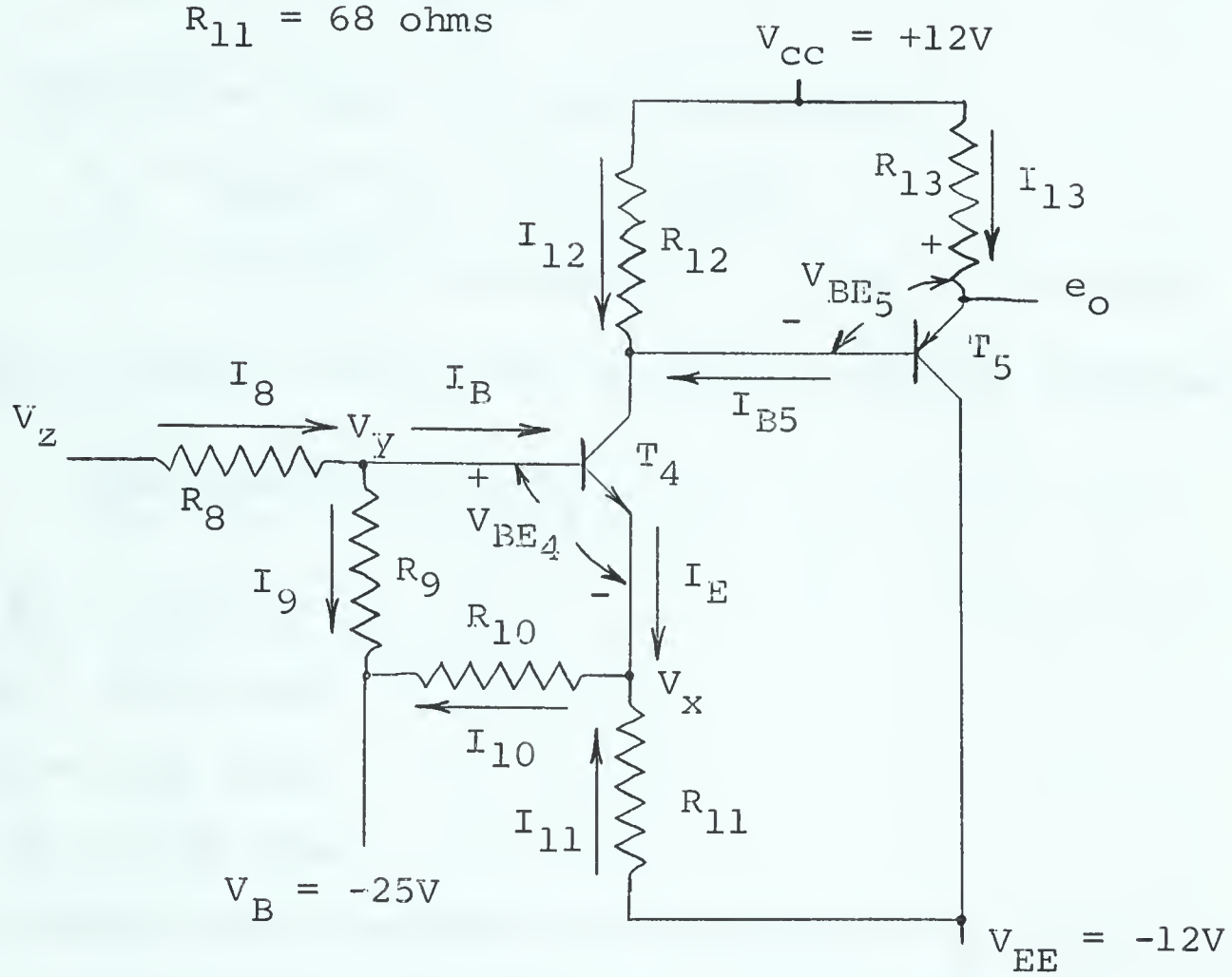


FIG. 27 SECOND STAGE OF GAIN IN OUTPUT AMPLIFIER

Let V_x = -14V and I_{10} = 30 ma.

To insure a minimum open loop gain of 1500 the voltage gain of T_4 was set at 50 to allow for attenuation in the resistor network R_8 - R_9.

$$A_v = \frac{h_{fb}R_{12}}{(h_{ib} + R_E)\ (1 + R_{12}h_{ob})} \quad (5) \quad \text{where } R_E = \frac{R_{10}\ R_{11}}{R_{10} + R_{11}}$$

For a 2N929 transistor and the same parameters used in the input stage the calculated value for R_{12} is 8.8K ohms.

Let R_{12} = 10K ohms.

The value of V_x can now be checked by assuming

$$I_E = I_{12} = \frac{V_{CC} - V_{BE_5}}{R_{12}}$$

The calculated value of V_x is -14.15 volts.

$V_y = V_{BE_4} + V_x = -13.55$ volts.

V_z = collector voltage of T_2 - V_{BE_3} = 3.4 volts.

If I_8 is greater than 1 ma, I_B can be ignored, therefore:

$$\frac{R_8(V_z - V_B)}{R_8 + R_9} = V_z - V_y$$

and $R_8 = 1.49\ R_9$

If R_8 = 8.2K ohms

R_9 = 5.5K ohms

Let R_9 = 5.6K ohms

The minimum input impedance at the base of T_4 is (5)

$$R_{i4} = \frac{(h_{ib} + R_E)(1 + R_{12}h_{ob})}{h_{ob}R_{12} + 1 + h_{fb}} \quad \text{where } R_E = \frac{R_{10}R_{11}}{R_{10} + R_{11}}$$

$$\frac{h_{ib} + R_E}{1 + h_{fb}}$$

8K ohms for $h_{ib_{min}}$ = 30 ohms

h_{fb} = 0.99

The minimum expected value of $R_8 + \frac{R_{i4}R_9}{R_{i4} + R_9}$ is approximately 12K ohms. To insure a minimum input impedance of 0.5 megohms at the base of T_3, R_7 was chosen as 10K ohms.

The maximum output impedance at the collector of T_4 is (5)

$$R_{04} = \frac{h_{ib} + R_E + R_g(1 + h_{fb})}{h_{ob}(h_{ib} + R_E + R_g) - h_{rb}h_{fb}}$$

for h_{ib} = 30 ohms

R_E = 56 ohms

R_g = 3.3K ohms

$h_{ob} = 2.5 \times 10^{-8}$

$h_{rb} = 4 \times 10^{-4}$

h_{fb} = 0.99

The calculated value of R_{04} is approximately 10K ohms. Therefore, choose R_{13} equal to 2.2K ohms. T_5 is a general purpose 2N1309 transistor.

RESULTS

The final decoder circuits are shown in Fig. 28, 29, 30, 31 and 32. The design component values which were changed and those components added to the circuits to obtain improved performance are marked with an asterisk.

Logic Block Data

(a) Input pulse requirements - The minimum amplitude of clock and code pulses for satisfactory operation is 3.5 volts. The code pulse amplitude must be no more than 1.5 volts smaller than the positive clock signal to insure satisfactory inhibit gate operation. The leading edge of the clock pulse must lag the leading edge of the code pulse. This delay should be no less than the rise time of the code pulse. The minimum clock pulse duration is 0.6 microseconds and the minimum code pulse width required is equal to the clock delay plus the clock pulse width and its fall time (Fig. 33).

(b) Switching characteristics - The switching times of the flip-flops with 4.5 volt clock and code pulses and a clock pulse rise time of 0.06 microseconds are;

$t_s = 0.25$ μsecs.

$t_f = 0.13$ μsecs.

$t_d = 0.30$ μsecs.

$t_r = 0.07$ μsecs.

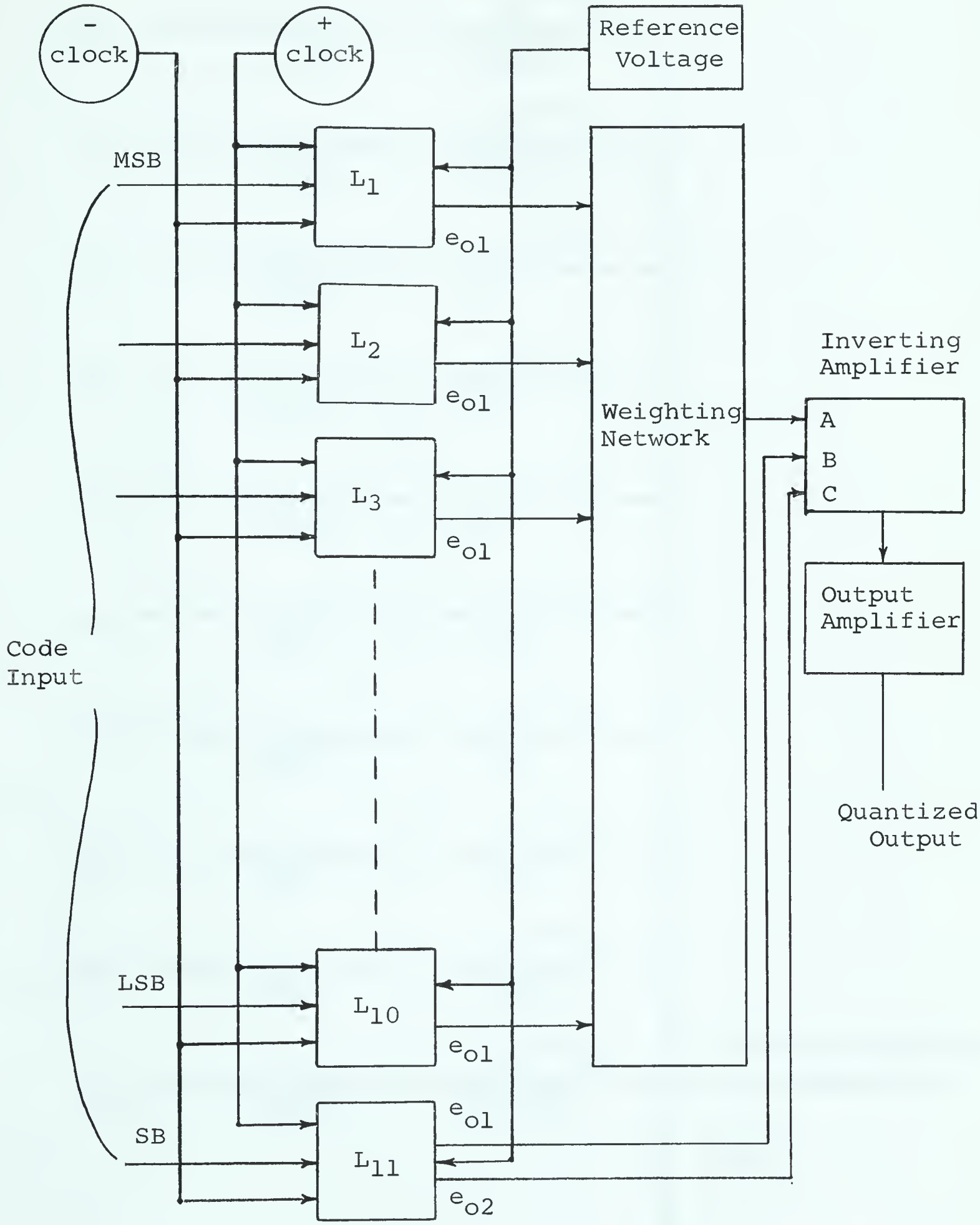


FIG. 28 DECODER BLOCK DIAGRAM

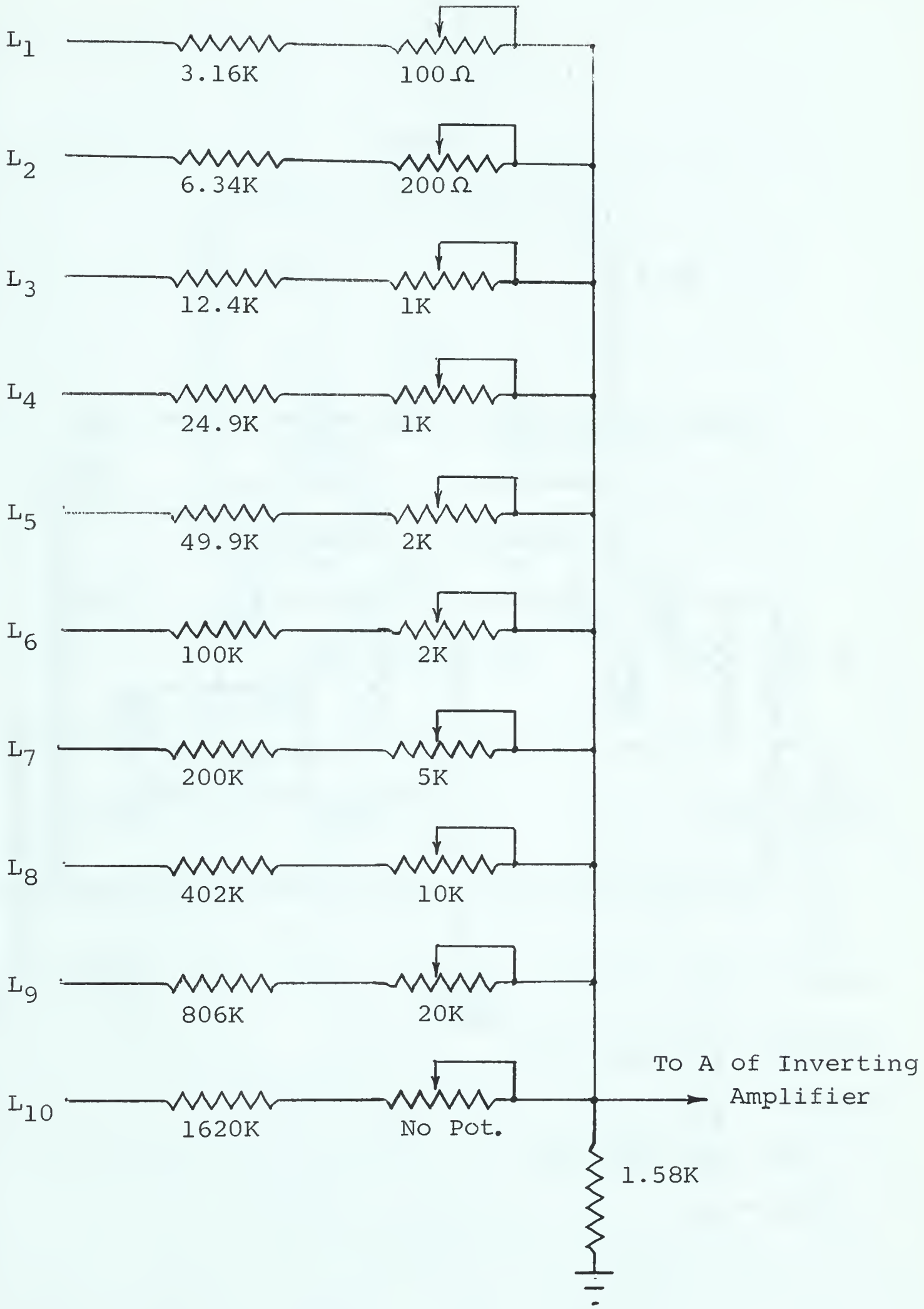
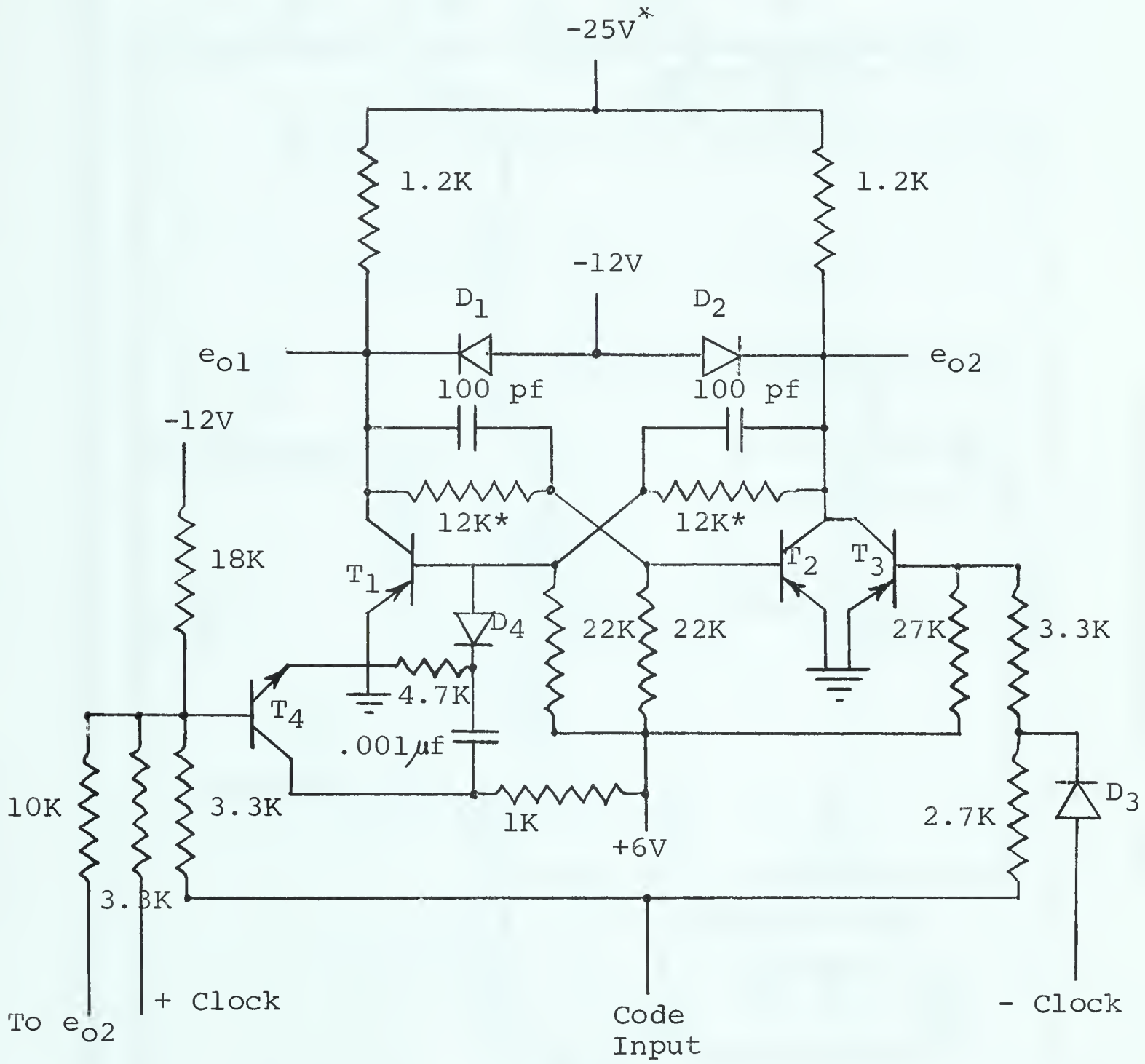


FIG. 29 WEIGHTING NETWORK



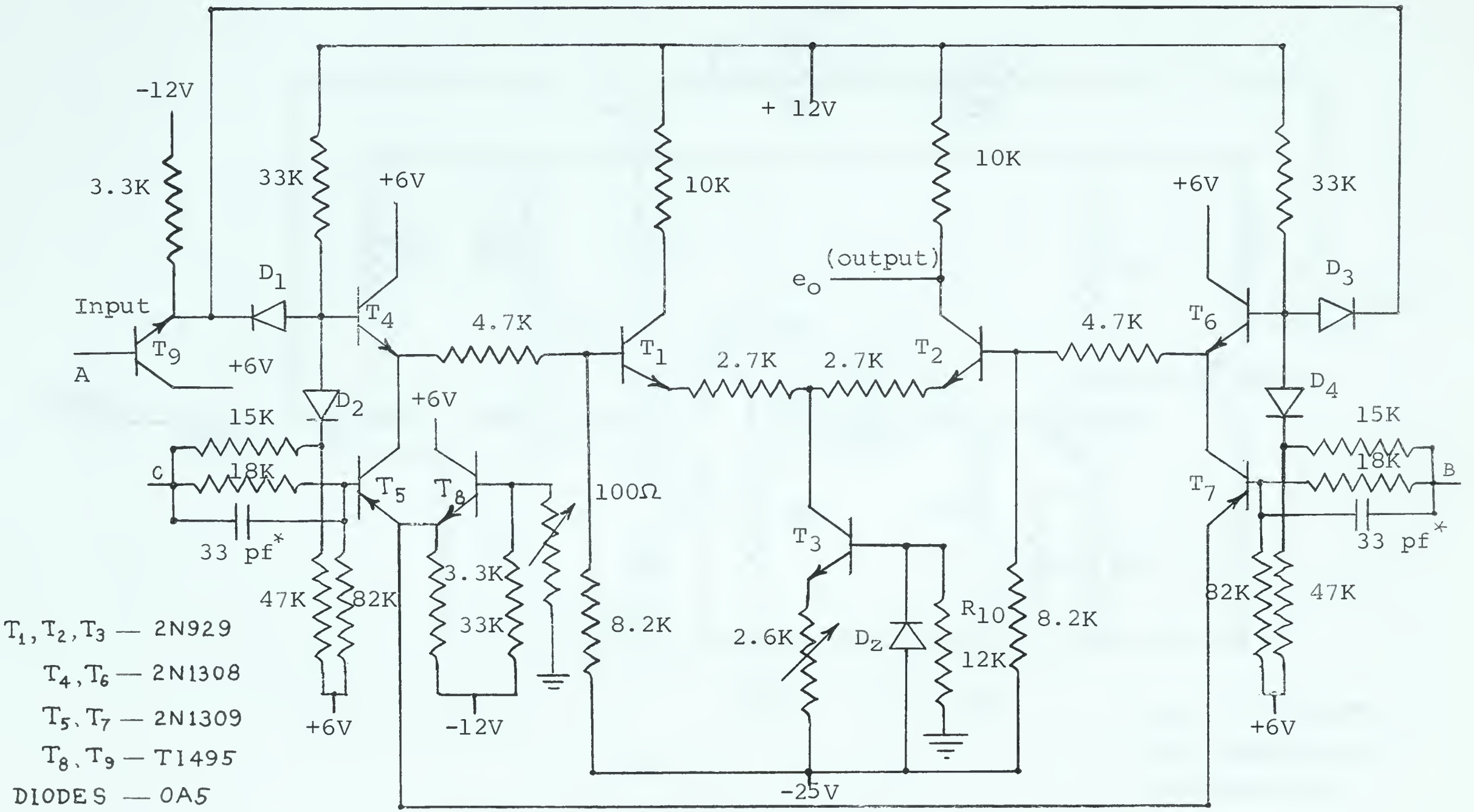
$T_1 = T_2 = T_3 = 2N1309$

$T_4 = 2N1308$

$D_2 = D_3 = D_4 = OA5$

$D_1 = OA10$

FIG. 30 LOGIC BLOCKS L_1 TO L_{11}



T_1, T_2, T_3 — 2N929

T_4, T_6 — 2N1308

T_5, T_7 — 2N1309

T_8, T_9 — T1495

DIODES — 0A5

D_Z — 6.5 V ZENER plus 2 - 1020 DIODES

R_{10} — PROVIDES TEMPERATURE COMPENSATION

FIG. 31 INVERTING AMPLIFIER

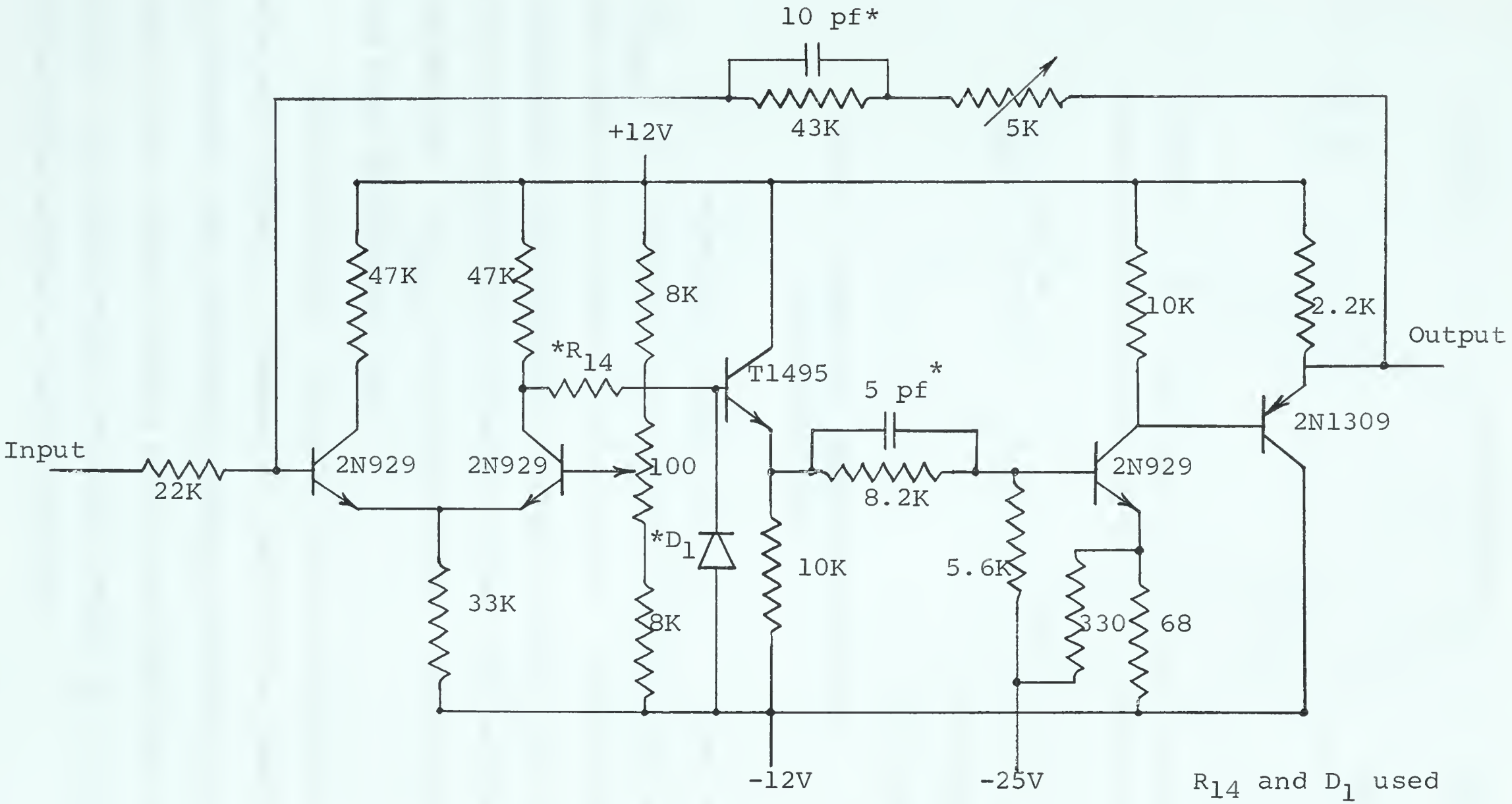


FIG. 32 OUTPUT AMPLIFIER

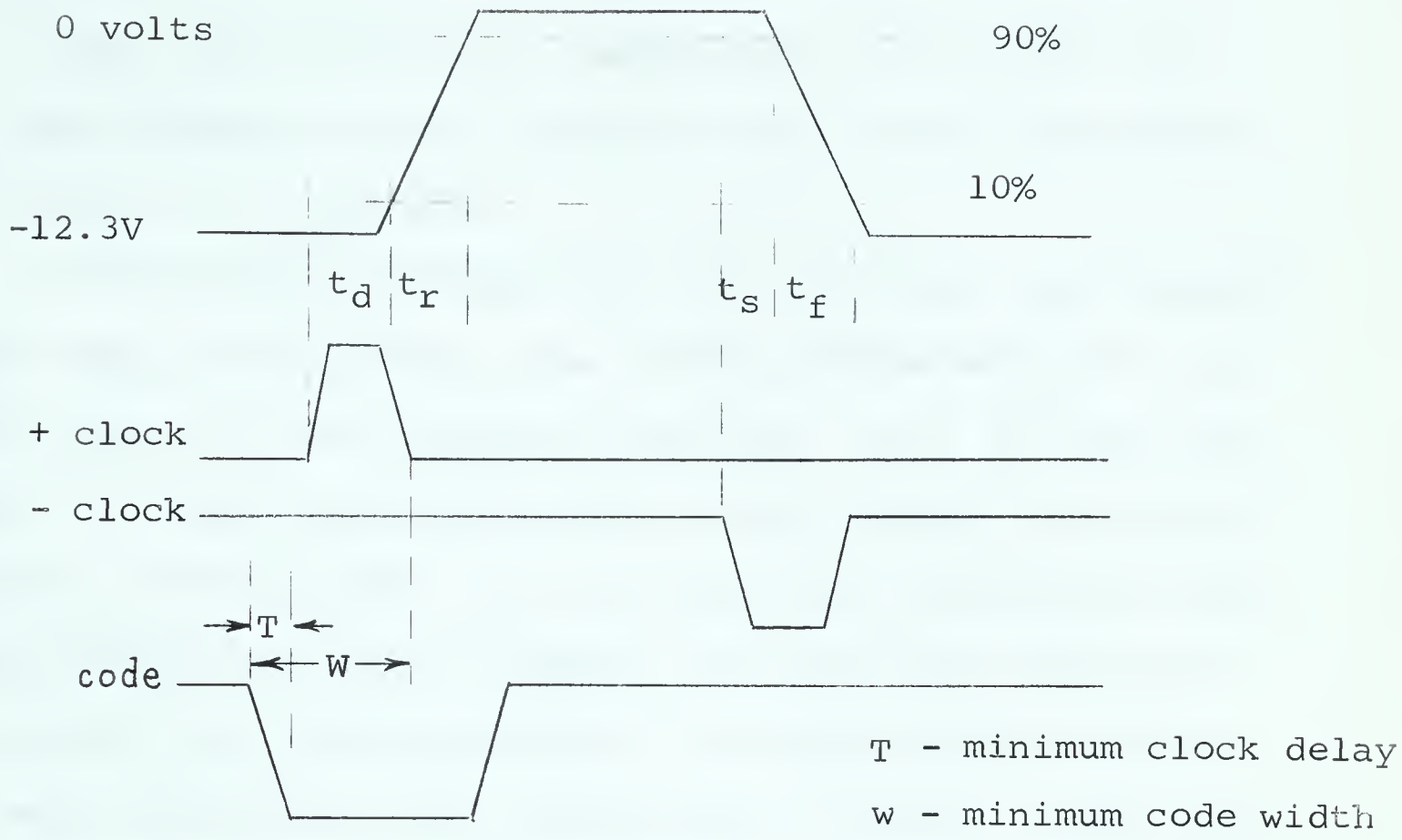


FIG. 33 SWITCHING CHARACTERISTICS OF THE FLIP-FLOPS

(c) Reference voltage stability - The "zero" state ($V_{CE_{sat}}$) is a function of collector current and temperature. This reference voltage increases by 0.1 millivolts per degree centigrade. The saturation voltage changes less than 0.3 millivolts because of collector current changes when used in the decoder. $V_{CE_{sat}}$ is matched within 2 millivolts for the five most significant bits.

The "one" state reference varies directly as the reference power supply. A number of tests of ten hours duration on different days indicated a maximum variation of 3 millivolts in the supply voltage after a one half hour warm-up period. The power supply voltage changed by 6 millivolts during three months of daily operation.

Oven tests indicated a temperature coefficient for the clamp diodes of minus 1 millivolt per degree centigrade when tested in a flip-flop.

The reference voltage from the flip-flops also depends on the load it must drive. The loading characteristics are shown in Fig. 34 for a typical flip-flop. Fig. 35 gives the change in voltage at the flip-flop output versus the desired weighting network output for the three most significant bits. Voltage variations due to loading the flip-flops are insignificant for the remaining bits. The clamp diodes for the five most significant bits are matched to within 2 millivolts of each other when the bit is in the "one" state and all other bits are"zero".

The regulation of the other flip-flop supplies is such that no appreciable change in the reference voltage occurs due to voltage variations in these supplies.

Weighting Network Data

It was rather difficult to obtain an exact value for the accuracy of the weighting network. To obtain some relative indication of the temperature effects, each bit output was measured at an ambient temperature of 23^{o} C and at 53^{o} C to obtain the output change due to resistor temperature coefficients. The results are shown in Table 3. Compared to other errors, these changes in the weighting network resistors cause no appreciable error.

LOADING CHARACTERISTICS
OF THE
DECODER FLIP - FLOPS
University of Alberta
August 3, 1964
FIGURE 34

DECREASE IN OUTPUT VOLTAGE (Millivolts)

32
28
24
20
16
12
8
4
0

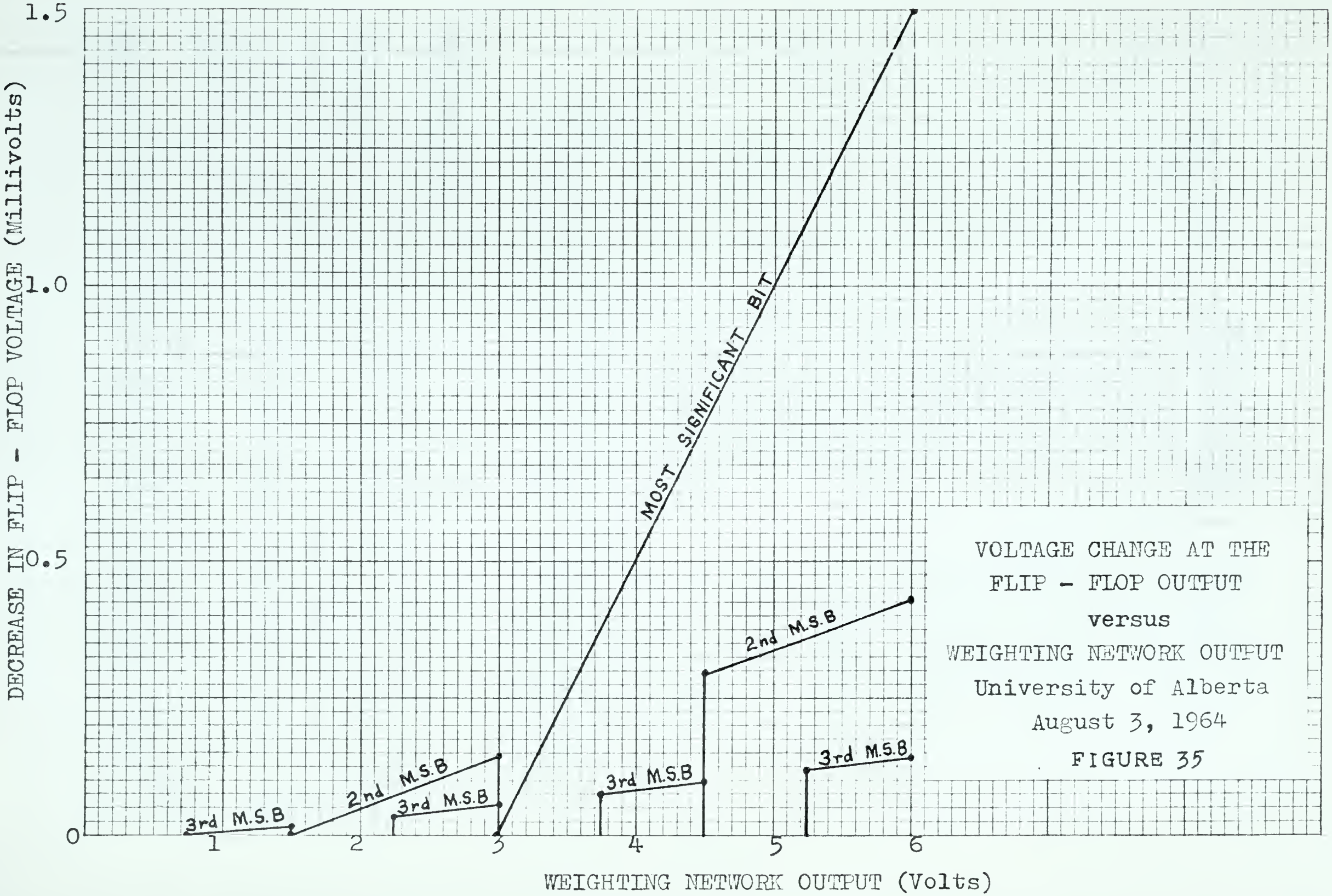
1 2 3 4 5 6

LOAD CURRENT (milliamperes)

X
Y
Z

a
b
c

a— Most significant bit (M.S.B.)
b— Second M.S.B.
c— Third M.S.B.
Note: The diodes are selected so that points X, Y, and Z are within 2 millivolts of each other.



VOLTAGE CHANGE AT THE
FLIP - FLOP OUTPUT
versus
WEIGHTING NETWORK OUTPUT
University of Alberta
August 3, 1964
FIGURE 35

Bit Number	Change in W.N. Output Voltage	Per cent change
MSB 1	-0.2 mv	1.7×10^{-4}
2	0.0 mv	0
3	+0.3 mv	1.0×10^{-3}
4	-0.3 mv	2.0×10^{-3}
5	-0.2 mv	2.8×10^{-3}
6	-0.05 mv	1.4×10^{-3}
7	0.00 mv	0
8	0.05 mv	5.5×10^{-3}
9	0.00 mv	0
LSB 10	0.00 mv	0

TABLE 3

Note: The measurements were taken to the nearest 0.1 millivolts for the five most significant bits and to the nearest 0.05 mv for the remaining bits.

Amplifier Data

The switching amplifier and output amplifier will be considered as a single unit for the data given unless stated otherwise. Amplifier drift will be considered on the basis of drift at the output as this will be more meaningful when considering errors.

The zero output drift of the differential amplifier and the output amplifier can be controlled over a small

temperature range by the proper choice of resistors (Figs. 31, 32). The major source of drift is due to the diode and transistor mismatch in the inverting amplifier switches, therefore the output drift was checked with the switches in the positive output mode and also in the negative output mode. Over an ambient temperature range of 22° C to 35° C the drift for the switch in the negative mode was plus 1 millivolt and with the switch set for positive outputs the drift was approximately minus 2 millivolts. This temperature effect is shown in Fig. 36 for all bits in the zero state except the sign bit.

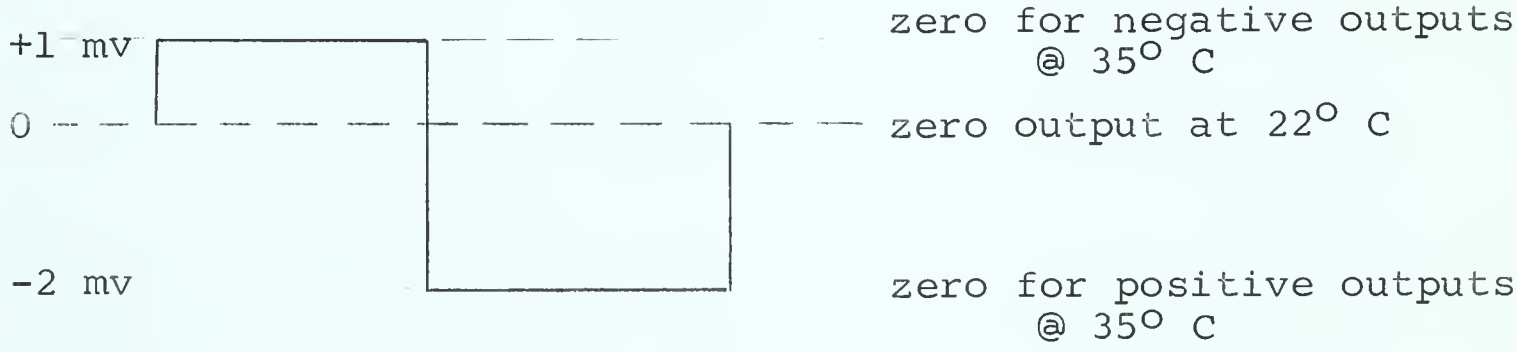


FIG. 36 EFFECT OF TEMPERATURE ON THE ZERO POINT

Typical output drift over a six hour period under laboratory conditions is shown in Fig. 37. The rise time for a 10 volt signal change is 1 microsecond from 5% to 95% of its final value.

The maximum output noise is 2 millivolts RMS. Practically all of the noise is power supply ripple.

The static voltage output from the decoder for a number of code combinations is given in Table 4.

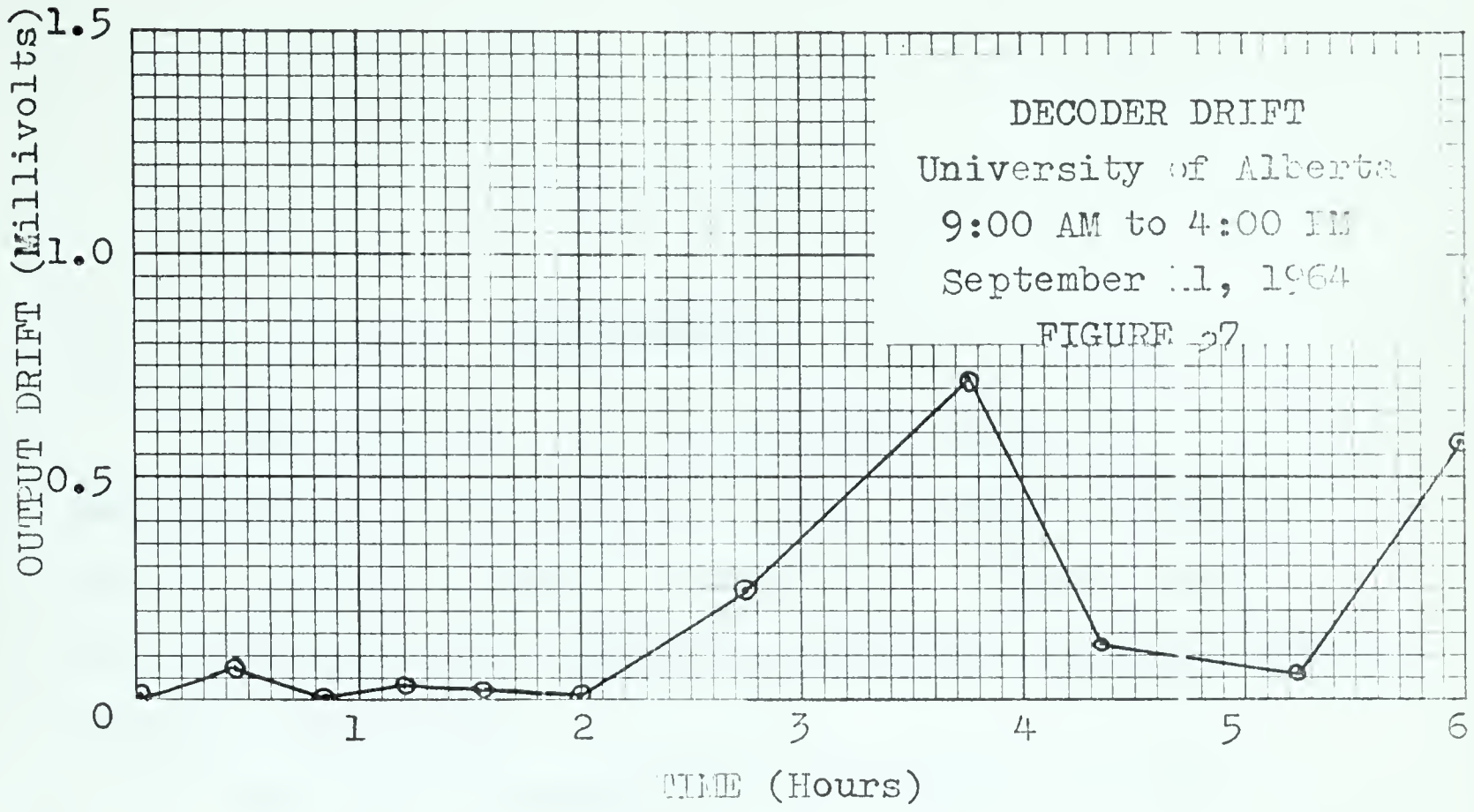
Summary of Significant Errors

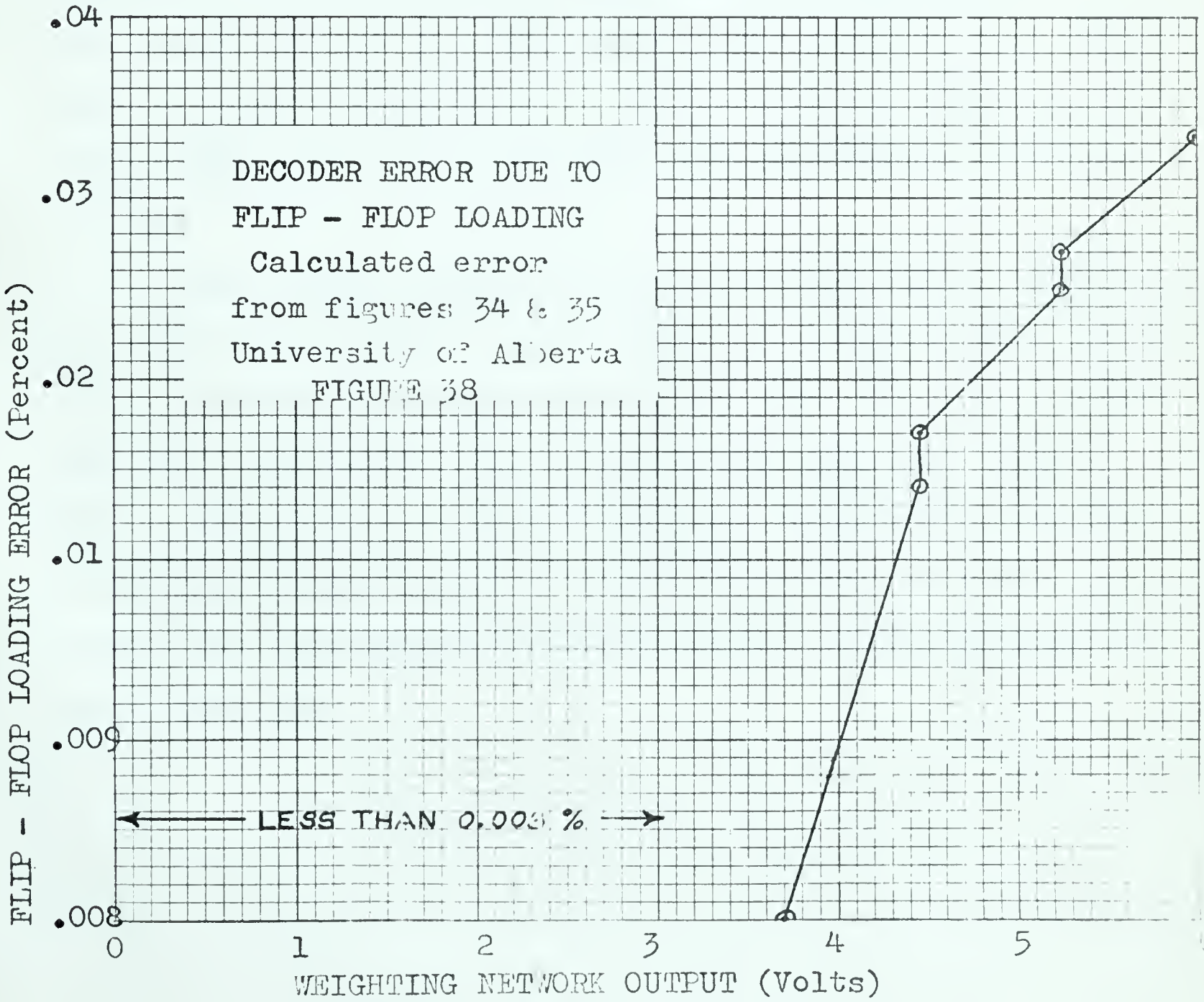
Reference power supply	±0.016% max.
Flip-flop loading (Fig. 38)	less than 0.035%
Clamp diodes	-0.008%/°C
Weighting network (Table 3)	less than 0.005%/°C
Zero drift	positive outputs ≤ -.2 mv/°C
	negative outputs ≤ +.2 mv/°C
Noise	2 mv RMS

Desired Output Voltage	Positive Output Voltage	Negative Output Voltage
0.000	0.000	0.000
0.010	0.010	0.010
0.050	0.050	0.050
0.200	0.200	0.200
0.500	0.501	0.501
1.000	0.999	0.999
2.000	2.001	2.001
3.000	3.002	3.003
4.000	4.004	4.004
5.000	5.002	5.002
6.000	6.007	6.007
7.000	7.006	7.005
8.000	8.005	8.006
9.000	9.003	9.004
10.000	10.000	10.001

Note: Readings taken to the nearest millivolt

TABLE 4 DECODER STATIC OUTPUT VOLTAGES


DECODER DRIFT
University of Alberta
9:00 AM to 4:00 PM
September 11, 1964
FIGURE 37
OUTPUT DRIFT (Millivolts)
1.5
1.0
0.5
0
1
2
3
4
5
6
TIME (Hours)


DECODER ERROR DUE TO
FLIP - FLOP LOADING
Calculated error
from figures 34 & 35
University of Alberta
FIGURE 38
FLIP - FLOP LOADING ERROR (Percent)
.04
.03
.02
.01
.009
.008
LESS THAN 0.003 %
0
1
2
3
4
5
WEIGHTING NETWORK OUTPUT (Volts)

CONCLUSIONS

The objective of constructing a relatively accurate ten bit binary decoder for use over a limited temperature range has been achieved. Although the decoder operates satisfactorily under laboratory conditions, some improvements could be considered.

The drift introduced by the switches in the inverting amplifier can be reduced, if required, by better matching of the switch components. This temperature drift may not introduce any appreciable error if the drift is such that it stays within the region of a guantized step represented by a given voltage.

The loading effects of the flip-flops can be eliminated by using the weighting network resistors as the summing resistors of a high gain operational amplifier. The clamp diodes can then be matched at the constant load they must supply. If the flip-flops are then temperature compensated, the most significant errors would be introduced by the reference power supply and the temperature coefficients of the weighting network resistors.

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APPENDIX A

Test Equipment

All voltage measurements were obtained with a John Fluke, Model 801, Differential D.C. Voltmeter and a John Fluke, Model 803, Differential DC-AC Voltmeter.

A Tektronix, Type 561-A oscilloscope with a Type 3A-1 plug in unit was used to observe wave forms.

Clock pulses were obtained from a General Radio Unit Pulse Generator, Type No. 1217-B and ~~clock~~ code pulses from a counter built with Philips flip-flop modules, No. B8 920 00.

To obtain the required delay between clock and code signals the circuit shown in Fig. 39 was used.

Transistor h- parameters used for calculations were measured on a Tektronix Type 575 Transistor-Curve Tracer.

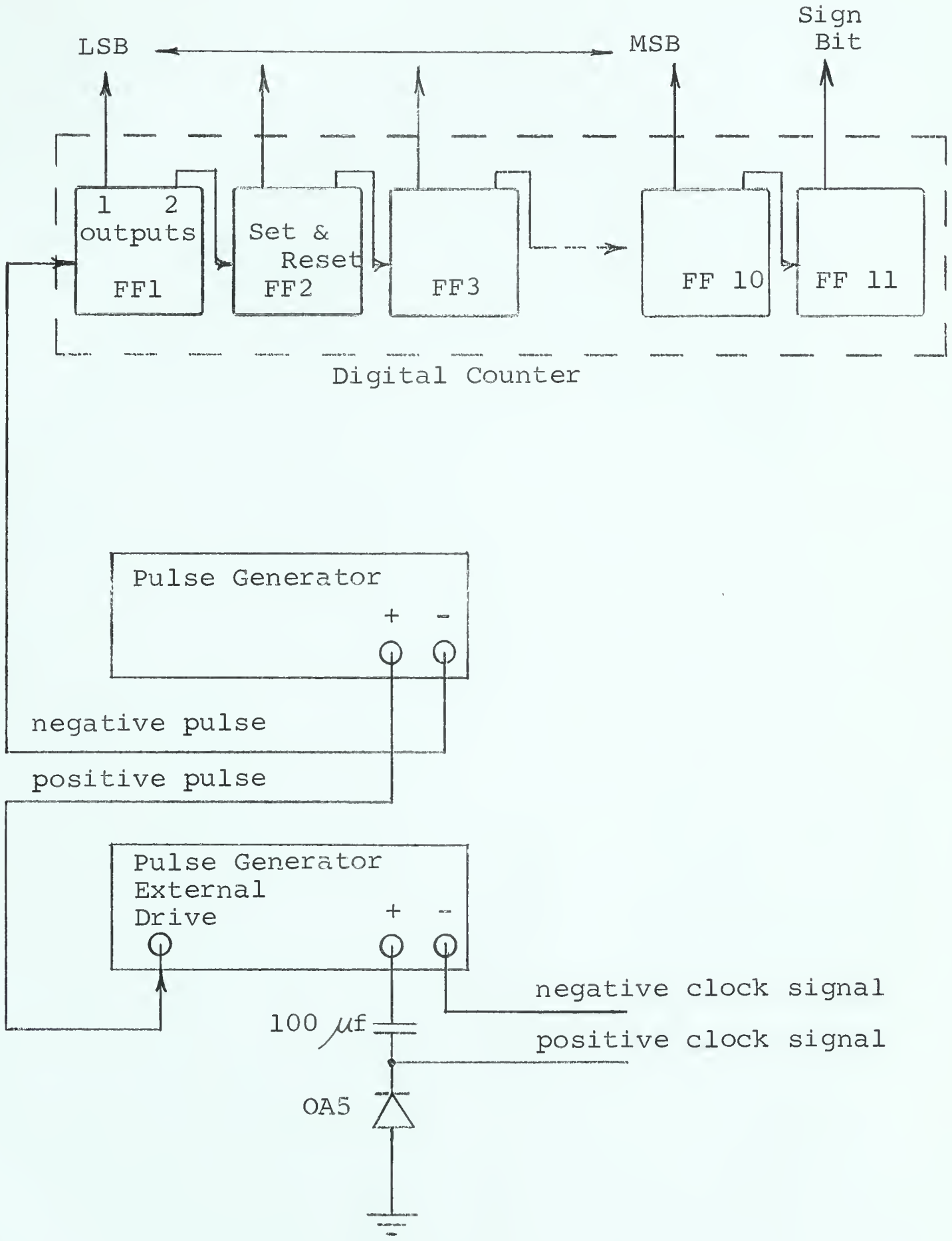

FIG. 39 TEST SET FOR CLOCK AND CODE PULSES